Blackfin®
Embedded Processor

Preliminary Technical Data

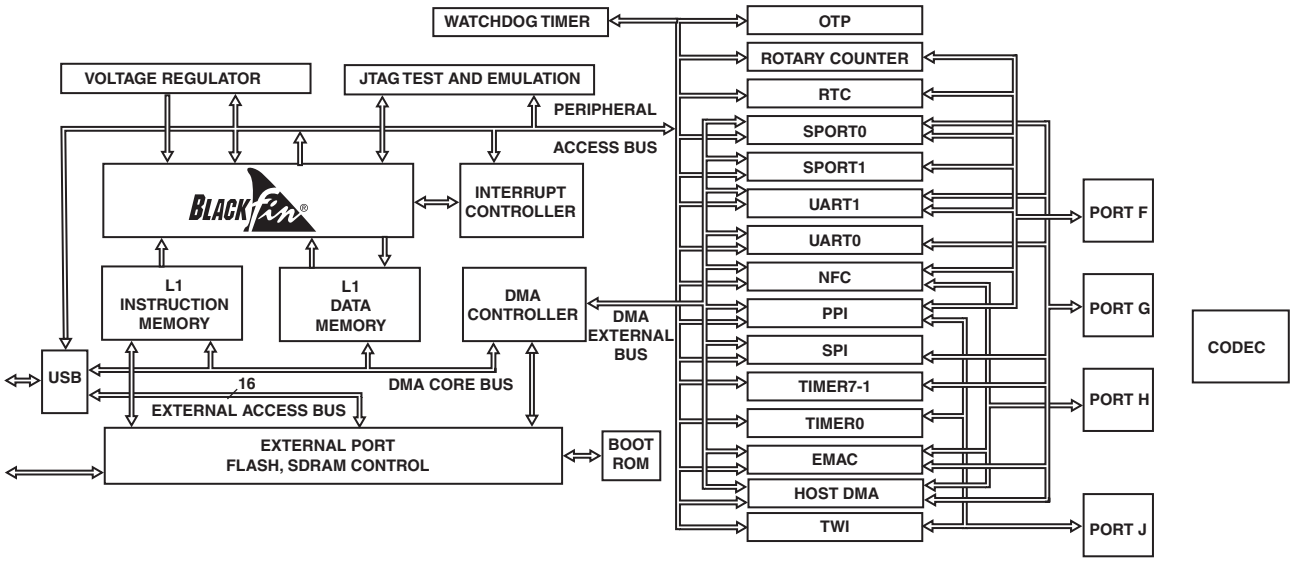
ADSP-BF523C/ADSP-BF525C/ADSP-BF527C

PROCESSOR FEATURES

- Up to 600 MHz high-performance Blackfin processor
  - RISC-like register and instruction model for ease of programming and compiler-friendly support
  - Advanced debug, trace, and performance monitoring
- tbd V to tbd V core V_{DD} with on-chip voltage regulation
- 1.8 V, 2.5 V, or 3.3 V I/O operation
- Embedded low power audio CODEC
- 289-ball MBGA package
- 132K bytes of on-chip memory
- External memory controller with glueless support for SDRAM and asynchronous 8-bit and 16-bit memories
- Nand flash controller
- Flexible booting options from external flash, SPI and TWI memory or from SPI, TWI, and UART host devices
- One-time programmable memory for security
- Two dual-channel memory DMA controllers
- Memory management unit providing memory protection
- See the published ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 Revision PrD datasheet for additional peripherals

EMBEDDED CODEC FEATURES

- Stereo 24-bit A/D and D/A converters
- Highly efficient headphone amplifier
- Complete stereo/mono or microphone/line interface
- Normal and USB modes programmed under software control
- Selectable ADC High Pass Filter
- TWI or SPI Interface
- Programmable Audio Data Interface Modes
- I^2S, Left, Right Justified or Frame Sync
- 16-/20-/24-/32-bit Word Lengths
- Master or Slave Clocking Mode
- Microphone Input and Electret Bias with Side Tone Mixer
- Audio sample rates
  - 8 kHz, 44.1 kHz or 88.2 kHz
    at XTI/CODEC_MCLK frequency of either 11.2896 MHz ($256 \times f_S$) or 16.9344 MHz ($384 \times f_S$)
  - 8 kHz, 32 kHz, 48 kHz or 96 kHz
    at XTI/CODEC_MCLK frequency of either 12.288 MHz ($256 \times f_S$) or 18.432 MHz ($384 \times f_S$)
- DAC
  - 100 dB (A-weighted) signal-to-noise ratio at 3.3 V
  - 95 dB (A-weighted) signal-to-noise ratio at 1.8 V
- ADC
  - 90 dB (A-weighted) signal-to-noise ratio at 3.3 V
  - 85 dB (A-weighted) signal-to-noise ratio at 1.8 V
- Low power
  - 8 mW stereo playback (1.8 V all power supplies)
  - 20 mW record and playback (1.8 V all power supplies))
- Low supply voltages
  - 1.8 V to 3.6 V analog supply range
  - 1.8 V to 3.6 V digital supply range



Rev. PrC

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REVISION HISTORY

6/08—Revision PrC: Changes from PrB to PrC

Adds extensive description of the CODEC peripheral.

6/07—Revision PrB: Changes from PrA to PrB

Corrects SS/PG and VRSEL 289-Ball Mini-BGA Ball Assignment (Alphabetically by Signal) 51

Corrects SS/PG and VRSEL 289-Ball Mini-BGA Ball Assignment (Numerically by Ball Number) 52

3/07—Revision PrA: Initial Version

GENERAL DESCRIPTION

This document describes the differences between the ADSP-BF523C/ADSP-BF525C/ADSP-BF527C and the ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 standard product. Please refer to the published ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 Revision PrD datasheet for general description and specifications. This document only describes the exceptions to that datasheet.

The ADSP-BF523C/ADSP-BF525C/ADSP-BF527C adds a low power stereo CODEC with an integrated headphone driver to the standard product. The CODEC is designed for portable MP3 audio/speech players and recorders. The CODEC is also suitable for MD, CD-RW machines and DAT recorders.

Stereo line and mono microphone level audio inputs are provided, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electret-type microphone.

CODEC DESCRIPTION

The CODEC in the ADSP-BF523C/ADSP-BF525C/ADSP-BF527C is a low power, high quality stereo audio CODEC for portable digital audio application. It features two 24-bit A/D converter channels and two 24-bit D/A converter channels.

In normal mode, the XMI/CODEC_MCLK oscillator is set up according to the desired sample rates of the ADC and DAC. For ADC or DAC sampling rates of 8 kHz, 32 kHz, 48 kHz or 96 kHz, CODEC_MCLK frequencies of either 12.288 MHz ($256 \times f_S$) or 18.432 MHz ($384 \times f_S$) can be used. For ADC or DAC sampling rates of 8 kHz, 44.1 kHz or 88.2 kHz, CODEC_MCLK frequencies of either 11.2896 MHz ($256 \times f_S$) or 16.9344 MHz ($384 \times f_S$) can be used.

In USB mode, the XTI/CODEC_MCLK frequency is only 12 MHz allowing for ADC and DAC sampling rates of 8 kHz, 44.1 kHz or 88.2 kHz.

The CODEC can operate with power supplies as low as 1.8 V for the analog port and 1.8 V for the digital port. The maximum voltage is 3.6 V for all power supplies.

The CODEC uses stereo 24-bit multi-bit sigma delta ADCs and DACs with oversampling digital interpolation and decimation filters. Digital audio input word lengths from 16-bits to 32-bits and sampling rates from 8 kHz to 96 kHz are supported.

Stereo audio outputs are buffered for driving headphones from a programmable volume control. Line level outputs are provided along with anti-thump mute and power-up/power-down circuitry.

The device is controlled by the ADSP-BF523C/ADSP-BF525C/ADSP-BF527C 2-wire (TWI) or 3-wire serial peripheral interface (SPI). The interface provides access to all features including volume controls, mutes, de-emphasis and extensive power management facilities.

The device is controlled by a TWI or SPI serial interface which provides access to all features including volume controls, mutes and extensive power management facilities.

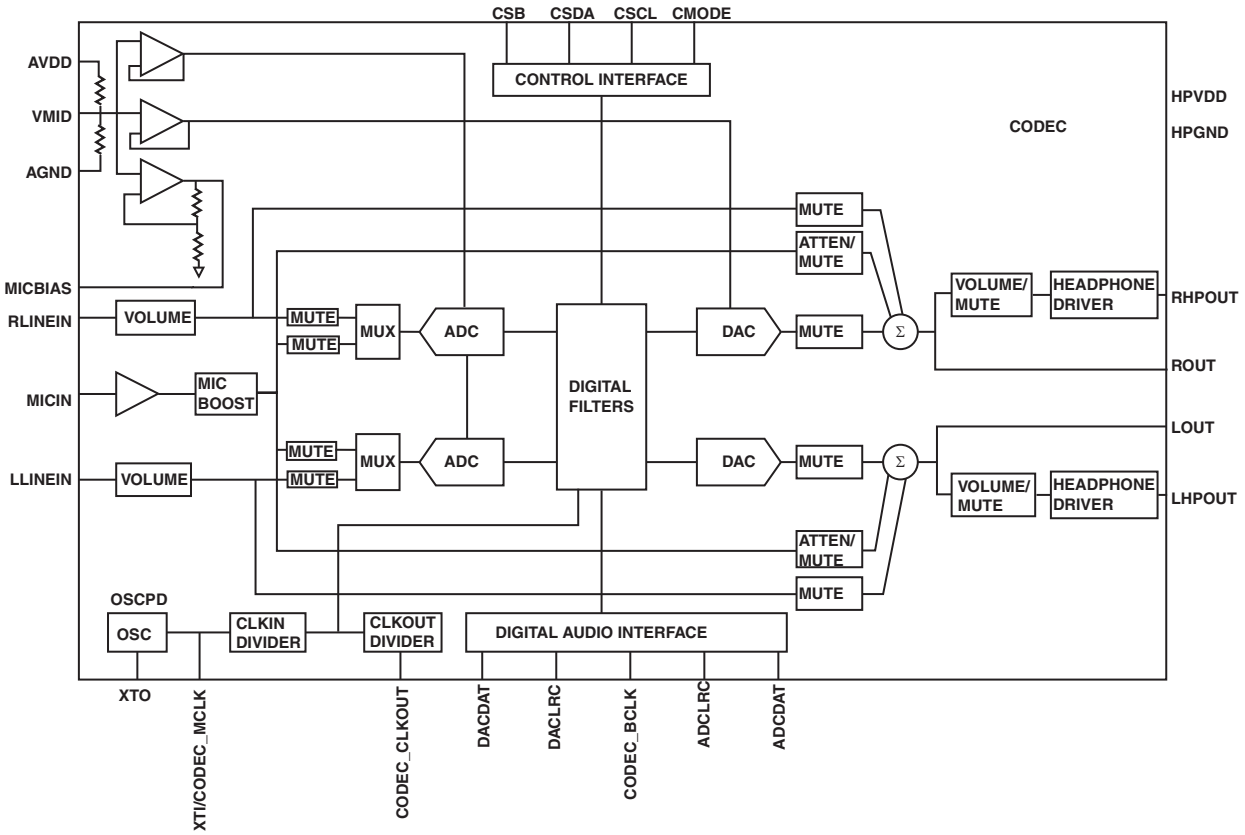

Figure 1. Audio CODEC Block Diagram

The CODEC is designed specifically for portable audio products. Its features, performance and low power consumption make it ideal for portable MP3 players and portable mini-disc players.

The CODEC includes line and microphone inputs to the on-board ADC, line and headphone outputs from the on-board DAC, a crystal oscillator, configurable digital audio interface and a choice of two or three wire control interface.

The CODEC includes three low noise inputs—a monaural microphone and left and right stereo lines. Line inputs have +12 dB to –34 dB logarithmic volume level adjustments and mute. The microphone input has –6 dB to +34 dB volume level adjustment. An electret microphone bias level is also available. All the required input filtering is contained within the device with no external components required.

The on-board stereo analog-to-digital converter (ADC) uses a high-quality multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption. The output from the ADC is available on the digital audio interface. The ADC includes an optional digital high pass filter to remove unwanted dc components from the audio signal.

The on-board digital-to-analog converter (DAC) accepts digital audio from the digital audio interface. Digital filter de-emphasis at 32 kHz, 44.1 kHz and 48 kHz can be applied to the digital data under software control. The DAC uses a high quality multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption.

The DAC outputs, microphone (SIDETONE) and line inputs (BYPASS) are available both at line level and through a headphone amplifier capable of efficiently driving low impedance headphones. The headphone output volume is adjustable in the analog domain over a range of +6 dB to –73 dB and can be muted.

The design of the CODEC has given much attention to power consumption without compromising performance. It includes the ability to power off selective parts of the circuitry under software control, thus conserving power. Nine separate power saving modes can be configured under software control including a standby and power-off mode.

Special techniques allow the audio to be muted and the device safely placed into standby, sections of the device powered off and volume levels adjusted without any audible clicks, pops or

zipper noises. Standby and power-off modes may be used dynamically under software control, whenever recording or playing is not required.

The device supports a number of different sampling rates including industry standard 8 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz and 96 kHz. Additionally, the device has an ADC and DAC that can operate at different sample rates.

There are two unique schemes featured within the programmable sample rates of the CODEC. Normal industry standard 256/384 × f_S sampling mode may be used, with the added ability to mix different sampling rates. A special USB mode is also included, where all audio sampling rates can be generated from a 12.00 MHz USB clock. Thus, for example, the ADC can record to the processor at 44.1 kHz and be played back from the CODEC at 8 kHz with no external digital signal processing required. The digital filters used for both record and playback are optimized for each sampling rate used.

The digitized output is available in a number of audio data formats I^2S, Frame Sync Mode (a burst mode in which frame sync plus two data packed words are transmitted), MSB-first, left justified and MSB-first, right justified. The digital audio interface can operate in both master or slave modes.

A crystal oscillator is included within the device. The device can generate the master clock or alternatively it can accept an external master clock.

AUDIO SIGNAL PATH

This section describes the signal flow, starting with the inputs, then the ADC/ADC filters, then the DAC filters/DAC, and finally the outputs.

Each section shows a diagram describing the circuit inside the CODEC, and a diagram showing the external components that must be connected to the CODEC pins. The external components are all shown together in Figure 2.

Line Inputs

The CODEC provides left and right channel line inputs (RLINEIN and LLINEIN). The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external high-fidelity or audio equipment.

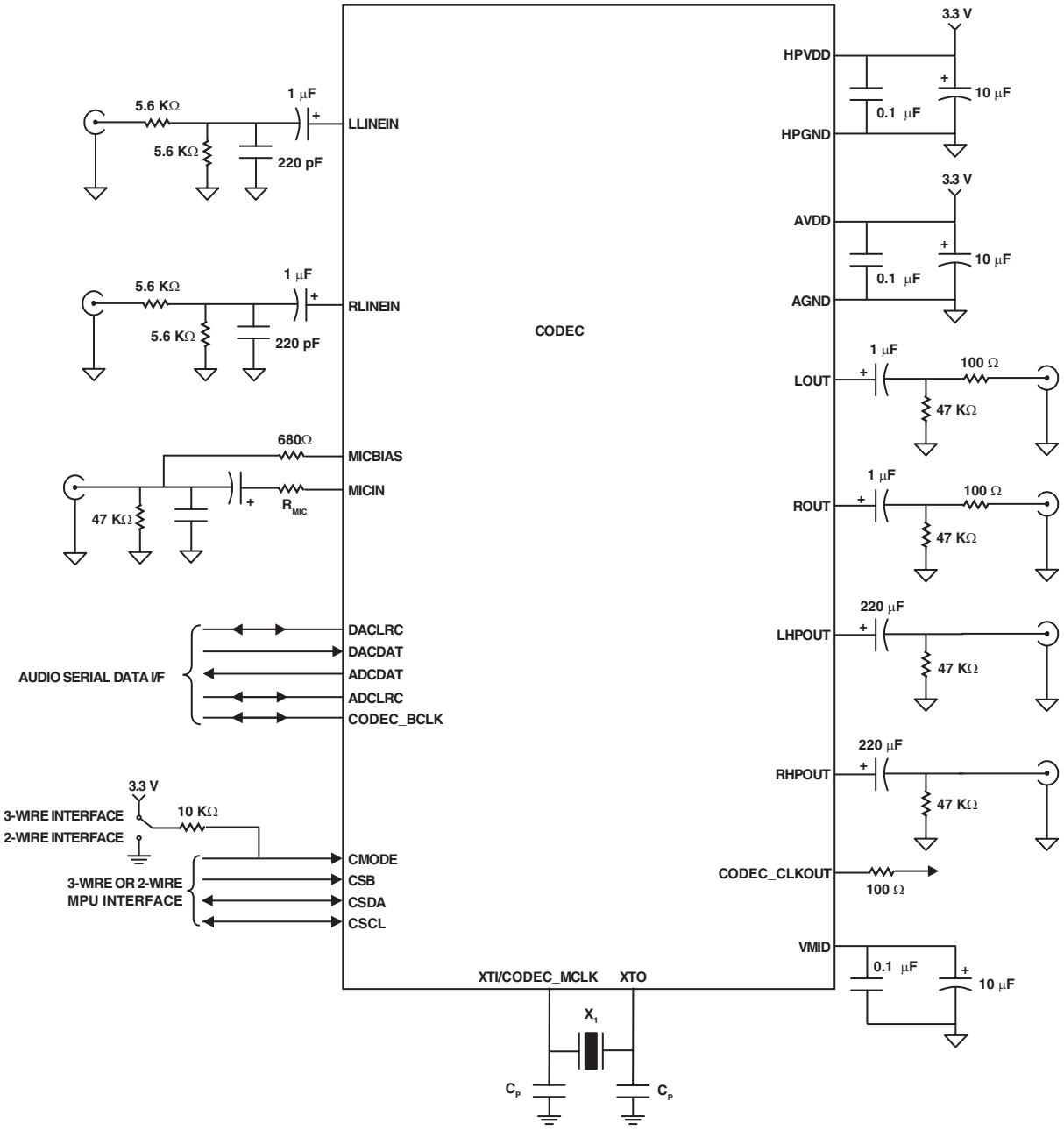

Figure 2. External Components Diagram

The external components needed to complete the line input application are shown in Figure 3.

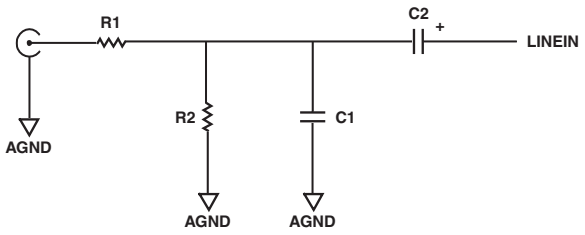

Figure 3. Line Input External Circuit

For interfacing to a typical CD system, it is recommended that the input be scaled to ensure that there is no clipping of the signal. R1 = 5.6 kΩ, R2 = 5.6 kΩ, C1 = 220 pF, C2 = 1 µF.

R1 and R2 form a resistive divider that attenuates the 2 V(rms) output from a compact disk player to a 1 V(rms) level to avoid overloading the inputs. R2 also provides a discharge path for C2, preventing the input to C2 from charging to an excessive voltage that could damage any connected equipment that is not suitably protected against high voltage. C1 forms an RF low pass filter for increasing the rejection of RF interference picked up on any cables. C2 blocks the dc path between the CODEC and the driving audio equipment. C2 together with the input impedance of the CODEC form a high pass filter.

As shown in Figure 4 the line inputs are biased internally through the operational amplifier to VMID. Whenever the line inputs are muted or the device placed in standby mode, the line inputs are kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

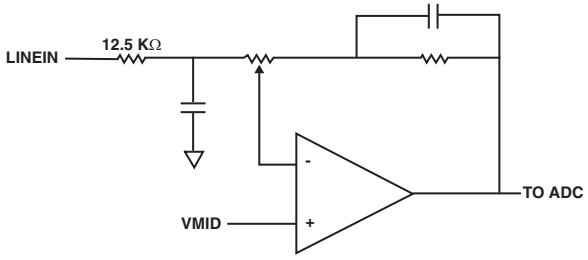

Figure 4. Line Input Internal Circuit

Both line inputs include independent programmable volume level adjustments and ADC input mute. Passive RF and active anti-alias filters are also incorporated within the line inputs to prevent degraded performance due to high frequency aliasing into the audio band.

LINMUTE/RINMUTE only mute the input to the ADC, which allows the line input signal to pass to the line output in bypass mode.

Using software control, the gain between the line inputs and the ADC is logarithmically adjustable from +12 dB to –34.5 dB in 1.5 dB steps. The ADC full scale input is 1.0 V(rms) at AVDD = 3.3 volts. Any voltage greater than full scale could overload the ADC and cause distortion. The full scale input tracks directly with AVDD. The gain is independently adjustable on both right and left line inputs. However, by setting the INBOTH bit while programming the volume control, both channels are simultaneously updated with the same value. Use of INBOTH reduces the number of software writes required. The line inputs to the ADC can be muted in the analog domain under software control. The software control registers are shown Table 1.

Microphone Input

MICIN is a high impedance, low capacitance input for connecting a wide range of monophonic microphones with different dynamics and sensitivities.

The MICIN includes programmable volume adjustments and a mute function. The scheme is shown in Figure 5. Passive RF and active anti-alias filters are incorporated within the microphone

Table 1. Line Input Software Control

Register Address	Bit	Label	Default	Description
000 0000 Left Line In	4:0	LINVOL[4:0]	10111 (0 dB)	Left Channel Line Input Volume Control 11111 = +12 dB in 1.5 dB steps down to 00000 = –34.5 dB
	7	LINMUTE	1	Left Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[4:0] and LINMUTE to RINVOL[4:0] and RINMUTE 0 = Disable Simultaneous Load
000 0001 Right Line In	4:0	RINVOL[4:0]	10111 (0 dB)	Right Channel Line Input Volume Control 11111 = +12 dB in 1.5 dB steps down to 00000 = –34.5 dB
	7	RINMUTE	1	Right Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[4:0] and RINMUTE to LINVOL[4:0] and LINMUTE 0 = Disable Simultaneous Load

inputs. These allow a matched interface to the multi-bit oversampling ADC and prevent high frequencies from aliasing into the audio band to degrade performance.

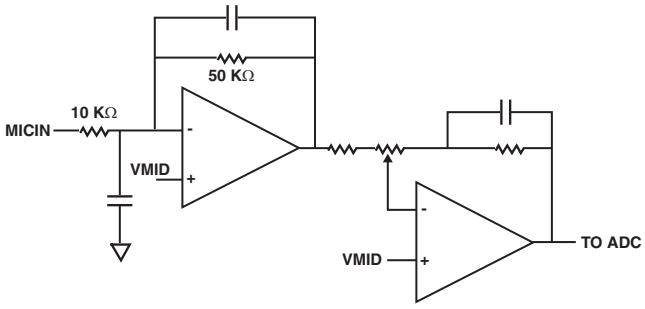

Figure 5. Microphone Input Internal Circuit

Software control for MICIN is shown in Table 2. The microphone mute only mutes the input to the ADC, which allows the microphone input signal to pass to the line output in sidetone mode.

Table 2. Microphone Input Software Control

Register Address	Bit	Label	Default	Description
000 0100	0	MICBOOST	0	Microphone Input Level Boost 1 = Enable Boost 0 = Disable Boost
	1	MUTEMIC	1	Microphone Mute to ADC 1 = Enable Mute 0 = Disable Mute

There are two stages of gain made up of two low noise inverting operational amplifiers.

The first stage has a nominal gain of G1 = 50 kΩ/10 kΩ = 5. The gain of the stage can be adjusted by adding an external resistor (R_{mic}) in series with MICIN (see Figure 6 on Page 9). The equation below can be used to calculate the gain versus R_{mic}.

Gain = 50 kΩ/(R_{mic} + 10 kΩ)

Or to calculate the value of Rmic to achieve a given gain:

R_{mic} = (50 kΩ/Gain)–10 kΩ

For example adding R_{mic} = 40 kΩ sets the gain of stage one to 1x (0 dB). For R_{mic} = 90 kΩ gain = 0.5 (–6 dB) and for R_{mic} = 0 gain = 5x (14 dB).

The internal 50 kΩ and 10 kΩ resistors have a tolerance of 15%.

The second stage has 0 dB gain that can be software configured to provide a fixed 20 dB of gain for low sensitivity microphones.

The microphone input can therefore be configured with a variable gain of between –6 dB and 14 dB on the first stage, and an additional fixed 0 dB or 20 dB on the second stage. This allows a total gain of –6 dB to 34 dB.

To maximize the signal-to-noise ratio, stage 1 and stage 2 gains should be configured so that the maximum signal that the ADC receives is equal to the full scale value. The ADC full scale input is 1.0 V(rms) at AVDD = 3.3 volts. Any voltage greater than full scale could overload the ADC and cause distortion. The full scale input tracks directly with AVDD.

The microphone input is biased internally through the operational amplifier to VMID. Whenever the line inputs are muted the MICIN input is kept biased to VMID using special anti-thump circuitry. This reduces audible clicks that may otherwise be heard when re-activating the input.

The microphone should be connected to the device as shown in Figure 6.

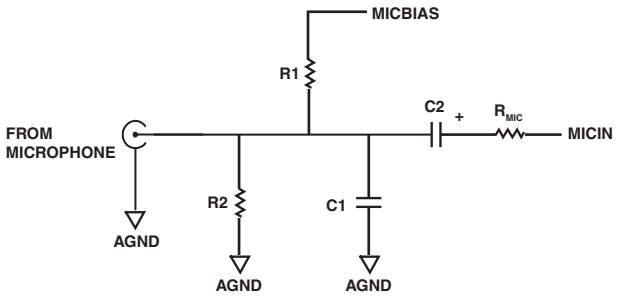

Figure 6. Microphone Input External Circuit

Recommended component values are C1 = 220 pF (npo ceramic), C2 = 1 µF, R1 = 680 Ω, R2 = 47 kΩ. R_{mic} values depend on the gain setting (see previous discussion).

R1 and R2 form part of the biasing network. R1 connected to MICBIAS is necessary only for electret type microphones that require a voltage bias. R2 should always be present to prevent the microphone input from charging to a high voltage which could damage the microphone upon connection. R1 and R2 should be large so as not to attenuate the signal from the microphone, which can have source impedance greater than 2 kΩ. C1 together with the source impedance of the microphone and the input impedance of MICIN forms an RF filter. C2 is a dc blocking capacitor that allows the microphone to be biased at a different dc voltage than the MICIN signal.

Microphone Bias

The MICBIAS output (shown in Figure 7) provides a low noise reference voltage suitable for biasing electret type microphones. The external resistor biasing network is shown in Figure 6, where MICBIAS is the output of the device (Figure 7).

There is a maximum source current capability of 3 mA available for the MICBIAS. This limits the smallest value of external biasing resistors that can safely be used.

The MICBIAS output is not active in standby mode.

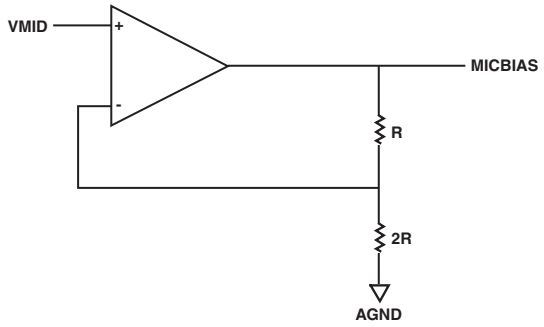

Figure 7. MICBIAS Internal Circuit

ADC

The CODEC uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated in the Figure 8. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

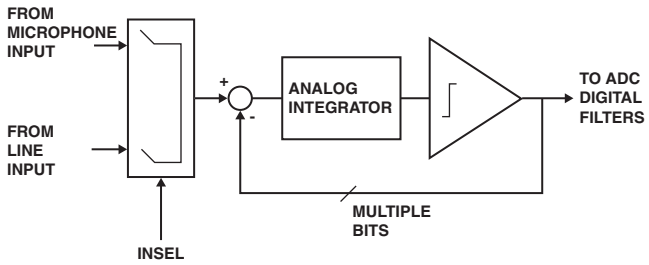

Figure 8. MultiBit Oversampling Sigma-Delta ADC

The ADC full scale input is 1.0 V(rms) at AVDD = 3.3 volts. Any voltage greater than full scale could overload the ADC and cause distortion. The full scale input tracks directly with AVDD.

The device uses a pair of ADCs. The input can be selected by software from either the line inputs or the microphone input. The two channels cannot be selected independently. The control is shown in Table 3.

The digital data from the ADC is fed for signal processing to the ADC filters.

Table 3. ADC Software Control

Register Address	Bit	Label	Default	Description
000 0100	2	INSEL	0	Microphone/Line Input Select 1 = Microphone Input Select 0 = Line Input Select

ADC Filters

The ADC filters perform true 24-bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. Figure 9 illustrates the digital filter path.

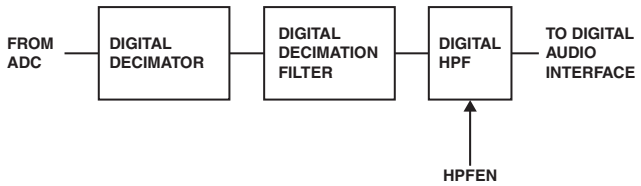

Figure 9. ADC Digital Filter

The ADC digital filters contain a digital high pass filter, selectable via software control. There are several types of ADC filters—frequency and phase responses of these are shown in

Digital Filter Characteristics on Page 39. The filter types are automatically configured depending on the sample rate chosen. See USB Mode Sample Rates on Page 23 more details.

When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR, the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the dc offset changes, the stored and subtracted value will not change unless the high-pass filter is enabled. The software control is shown in Table 4.

Table 4. ADC Software Control

Register Address	Bit	Label	Default	Description
000 0101	0	ADCHPD	0	ADC High Pass Filter Enable 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	4	HPOR	0	Store DC Offset When High Pass Filter Disabled 1 = Store Offset 0 = Clear Offset

DAC Filters

The DAC filters perform true 24-bit signal processing to convert the incoming digital audio data from the digital audio interface at the specified sample rate to multi-bit oversampled data for processing by the analog DAC. Figure 10 illustrates the DAC digital filter path.

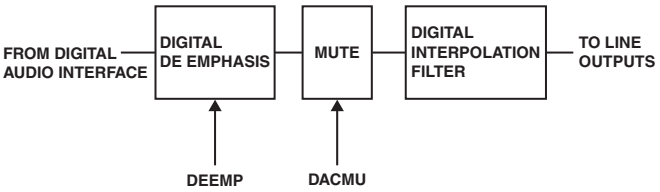

Figure 10. DAC Filter

The DAC digital filter can apply digital de-emphasis under software control, as shown in Table 5. The DAC can also perform a soft mute where the audio data is digitally brought to a mute level. This removes any abrupt step changes in the audio that might otherwise result in audible clicks in the audio outputs.

Table 5. DAC Software Control

Register Address	Bit	Label	Default	Description
000 0101	2:1	DEEMP[1:0]	00	De-emphasis Control (Digital) 11 = 48 kHz 10 = 44.1 kHz 01 = 32 kHz 00 = Disable
	3	DACMU	1	DAC Soft Mute Control (Digital) 1 = Enable Soft Mute 0 = Disable Soft Mute

DAC

The CODEC uses a multi-bit sigma-delta oversampling digital-to-analog converter as shown in Figure 11.

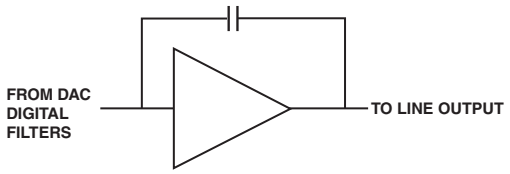

Figure 11. Multi-bit Oversampling Sigma Delta Schematic

The DAC converts the multi-level digital audio data stream from the DAC digital filters into high quality analog audio.

Line Outputs

The CODEC provides two low impedance line outputs LOUT and ROUT, suitable for driving line loads with 10 kΩ impedance and 50 pF capacitance. The line output is used to selectively sum the outputs from the DAC and/or the line inputs in bypass mode.

The LOUT and ROUT outputs are only available at a fixed line output level that is not adjustable in the analog domain. The level is fixed such that at the DAC full scale level the output is 1.0 V(rms) at AVDD = 3.3 volts. The DAC full scale level tracks directly with AVDD.

The internal circuit is shown in Figure 12. The line output includes a low order audio low pass filter for removing out-of band components from the sigma-delta DAC. Therefore no further external filtering is required in most applications.

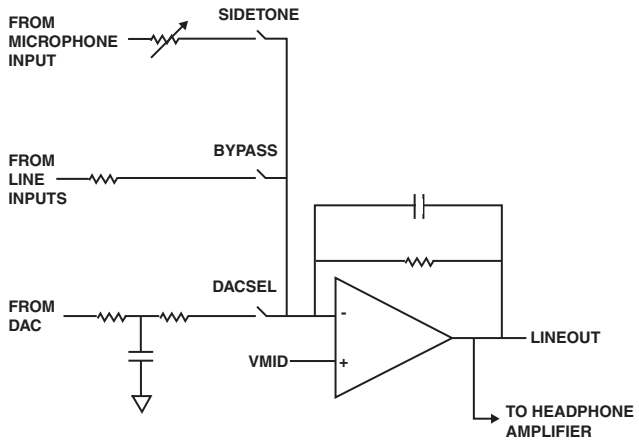

Figure 12. Line Output

The DAC output, line input and microphone are summed into the line output. In DAC mode only the output from the DAC is routed to the line outputs. In bypass mode the line input is summed into the line outputs. In sidetone mode the microphone input is summed into the line output. These features can

be used for either over-dubbing, or if the DAC is muted, as a pure analog bypass or sidetone feature that avoids any digital signal processing.

The line output is muted by either muting the DAC (analog) or soft muting (digital) and disabling the bypass and sidetone paths. See DAC Filters on Page 10 for more information. Whenever the DAC is muted or the device placed in standby mode, the dc voltage is maintained at the line outputs to prevent audible clicks.

The software control for the line outputs is shown in Table 6.

Table 6. Output Software Control

Register Address	Bit	Label	Default	Description
0000100	3	BYPASS	1	Bypass Switch 1 = Enable Bypass 0 = Disable Bypass
	4	DACSEL	0	DAC Select 1 = Select DAC 0 = Do Not Select DAC
	5	SIDETONE	0	Side Tone Switch 1 = Enable Side Tone 0 = Disable Side Tone

The recommended external components are shown in Figure 13 with C1 = 10 µF, R1 = 47 kΩ, R2 = 100 Ω.

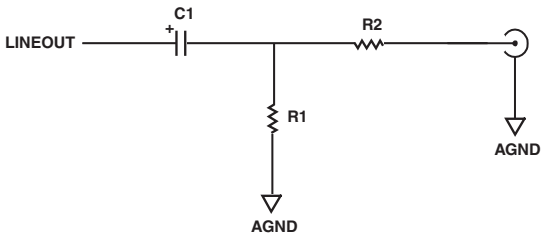

Figure 13. Line Outputs External Circuit

C1 forms a dc blocking capacitor to the line outputs. R1 prevents the output voltage from drifting to protect equipment connected to the line output. R2 forms a de-coupling resistor preventing abnormal loads from disturbing the device. Poor choice of dielectric material for C1 can have dramatic effects on the measured signal distortion at the output.

Headphone Amplifier

The CODEC has a stereo headphone output available on LHPOUT and RHPOUT. The output is designed for driving 16 Ω or 32 Ω headphones with maximum efficiency and low power consumption. The headphone output includes a high quality volume level adjustment and mute function.

The internal circuit is shown in Figure 14.

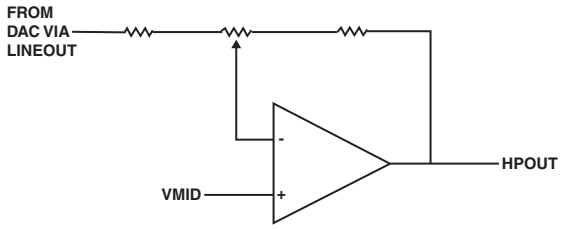

Figure 14. Headphone Amplifier

LHPOUT and RHPOUT volumes can be independently adjusted under software control using the LHPVOL[6:0] and RHPVOL[6:0] bits of the headphone output control registers. The adjustment is logarithmic with an 80 dB range in 1 dB steps from +6 dB to –73 dB.

The headphone outputs can be separately muted by writing codes less than 0110000 to the LHPVOL[6:0] or RHPVO[6:0] bits. Whenever the headphone outputs are muted or the device placed in standby mode, the dc voltage is maintained at the line outputs to prevent audible clicks.

A zero-cross-detect circuit is provided at the input to the headphones under the control of the LZCEN and RZCEN bits of the headphone output control register. Using these controls, the volume control values are only updated when the input signal to the gain stage is close to the analog ground level. This minimizes audible clicks and zipper noise as the gain values are changed or the device muted. This circuit has no time out, so if dc levels of more than approximately 20 mV are being applied to the gain stage input , the gain will not be updated. This zero-cross function is enabled when the LZCEN or RZCEN bit is set high during a volume register write. If there is concern that a dc level may have blocked a volume change (one made with LZCEN or RZCEN set high) then a subsequent volume write of the same value, but with the LZCEN or RZCEN bit set low will force a volume update, regardless of the dc level.

The LHPOUT and RHPOUT volume and zero-cross settings can be changed independently. Or the programmer can lock the two channels together, allowing both to be updated simultaneously. This halves the number of serial writes needed, provided that the gain is the same for both channels. Setting LRHPBOTH while writing to LHPVOL and LZCEN will simultaneously update the right headphone controls. Similarly, setting RLHPBOTH while writing to RHPVOL and RZCEN will simultaneously update the left headphone controls.

Software control is shown in Table 7.

Table 7. Headphone Output Software Control

Register Address	Bit	Label	Default	Description
000 0010	6:0	LHPVOL[6:0]	1111001 (0 dB)	Left Channel Headphone Output Volume Control +6 dB (1111111) in 1 dB steps down to –73 dB(0110000) 0000000 to 0101111 = MUTE
	7	LZCEN	0	Left Channel Zero-Cross Detect Enable 1 = Enable 0 = Disable
	8	LRHPBOTH	0	Simultaneous Load of Left Channel Volume, Mute and Zero-Cross Data to Right Channel 1 = Enable Simultaneous Load of LHPVOL[6:0] and LZCEN to RHPVOL[6:0] and RZCEN 0 = Disable Simultaneous Load
000 0011	6:0	RHPVOL[6:0]	1111001 (0 dB)	Right Channel Headphone Output Volume Control +6 dB (1111111) in 1 dB steps down to –73 dB(0110000) 0000000 to 0101111 = MUTE
	7	RZCEN	0	Right Channel Zero-Cross Detect Enable 1 = Enable 0 = Disable
	8	RLHPBOTH	0	Simultaneous Load of Right Channel Volume, Mute and Zero-Cross Data to Left Channel 1 = Enable Simultaneous Load of RHPVOL[6:0] and RZCEN to LHPVOL[6:0] and LZCEN 0 = Disable Simultaneous Load

The recommended external components are shown in Figure 15 with C1 = 220 µF (10 V electrolytic) and R1 = 47 kΩ.

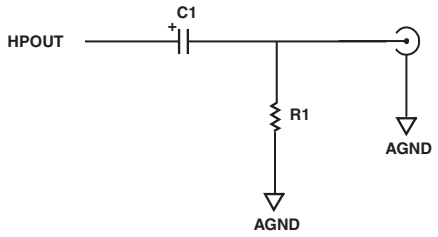

Figure 15. Headphone Output External Circuit

C1 is a dc blocking capacitor that isolates the dc of the HPOUT from the headphones. R1 is a pull-down resistor that discharges C1 to prevent damage to the headphones.

Bypass Mode

The bypass mode routes analog line inputs directly to the analog line and headphone outputs as shown in Figure 16.

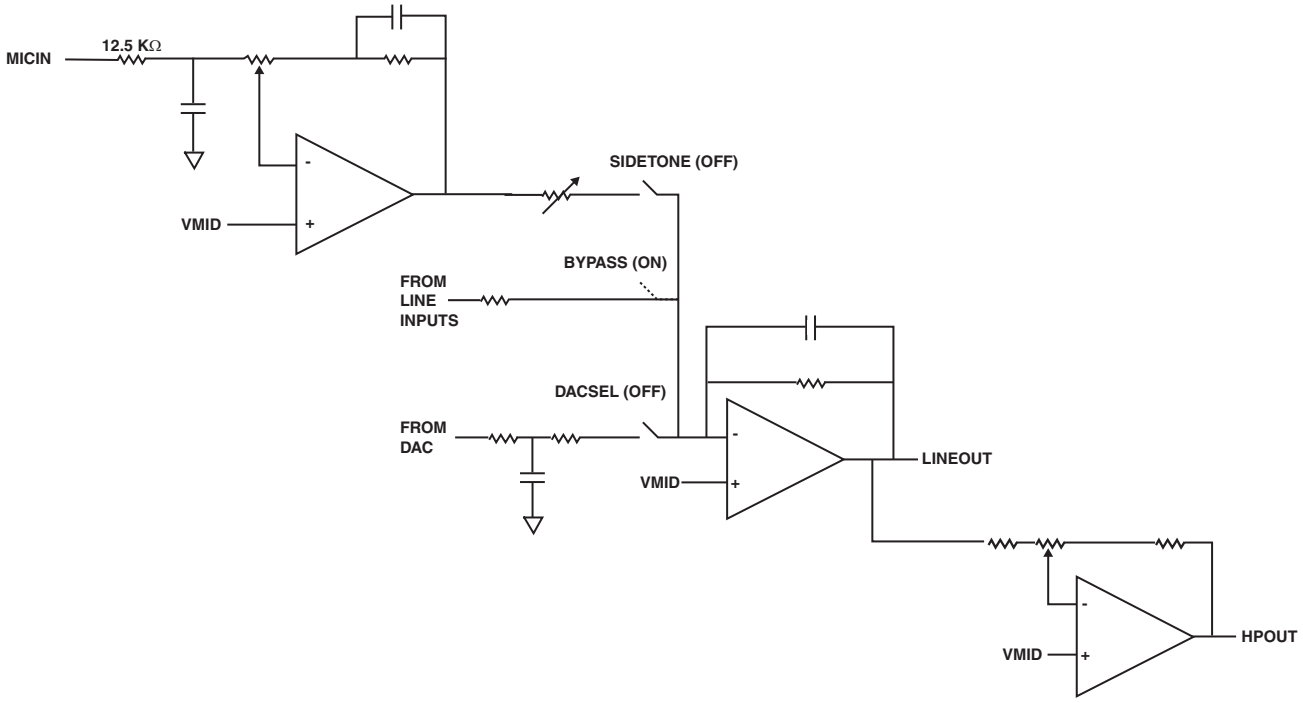

Figure 16. Signal Routing in Bypass Mode

Bypass mode is selected under software control using the BYPASS bit as shown in Table 8. In true bypass mode, the output from the DAC (DACSEL) and (SIDETONE) should be deselected from the line output block. However this can also be used to sum the DAC output, line inputs together and microphone inputs. The analog line input and headphone output volume controls and mutes are still operational in bypass mode. The 0 dB gain setting is recommended for the line input volume control to avoid distortion. The maximum signal at any point in the bypass path must be no greater than 1.0 V(rms) at AVDD = 3.3 V. This level tracks directly with AVDD. This means that if the DAC is producing a 1 V(rms) signal, and it is being summed with a 1 V(rms) line BYPASS signal, the resulting LINEOUT signal will be clipped.

Table 8. Bypass Mode Software Control

Register Address	Bit	Label	Default	Description
000 0100	3	BYPASS	1	Bypass Switch (analog) 1 = Enable Bypass 0 = Disable Bypass

Sidetone Mode

The sidetone mode routs the microphone input to the line and headphone outputs as shown in Figure 17.

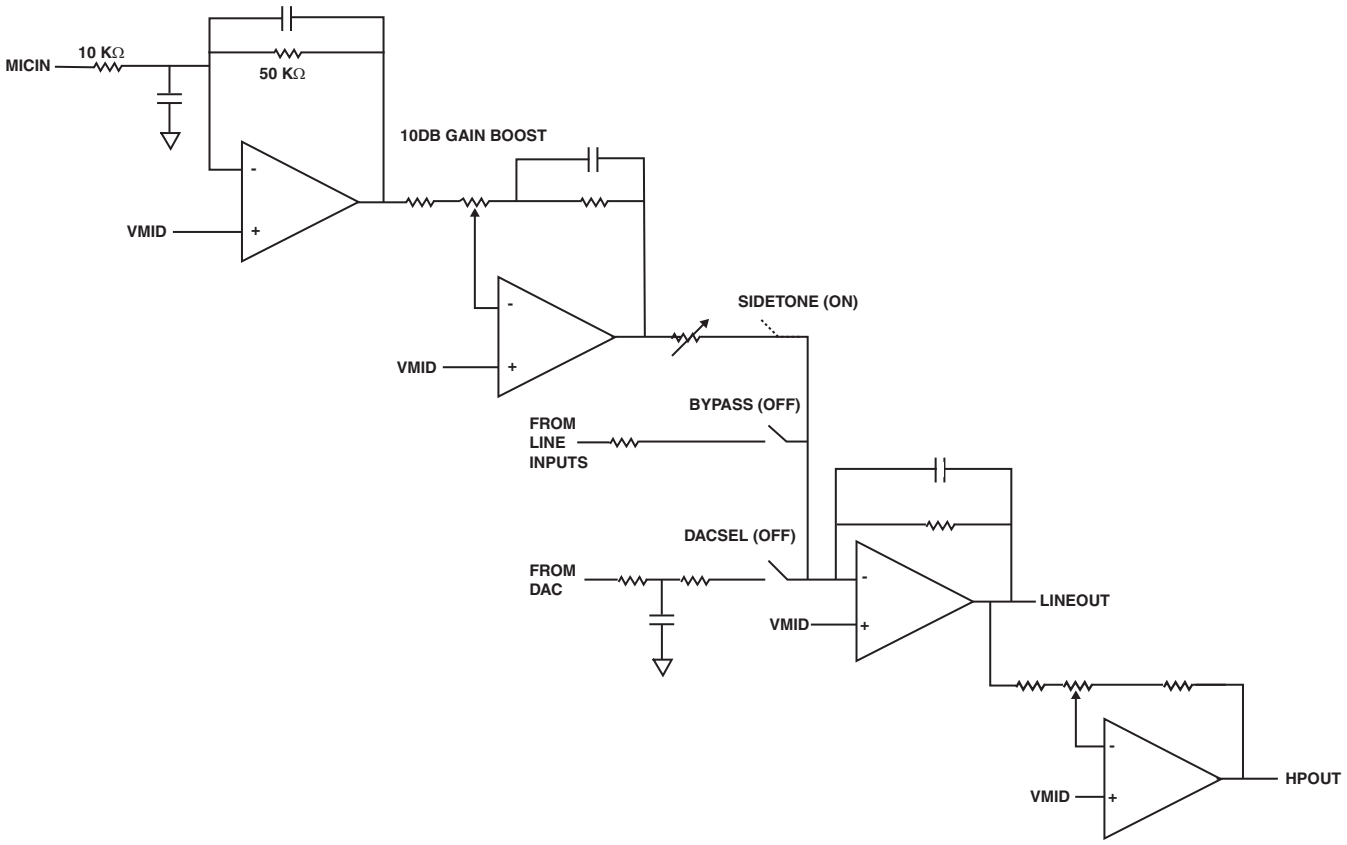

Figure 17. Sidetone Mode

The sidetone mode allows the microphone input to be attenuated to the outputs for telephone and headset applications.

The sidetone mode and attenuation are selected under software control using the SIDETONE bit as shown in Table 9. In true sidetone the output from the DAC (DACSEL) and line inputs (BYPASS) should be deselected from the line output block. However, this can also be used to sum the DAC output, line inputs and microphone inputs together. The microphone boost gain control and headphone output volume control and mutes are still operational in sidetone mode. To avoid distortion the maximum signal at any point in the sidetone path must be no greater than 1.0 V(rms) at AVDD = 3.3V. This level tracks directly with AVDD.

Table 9. Sidetone Mode Control

Register Address	Bit	Label	Default	Description
000 0100	5	SIDETONE	0	Sidetone Switch (analog) 1 = Enable Side Tone 0 = Disable Side Tone
	7:6	SIDEATT[1:0]	00	Sidetone Attenuation 11 = –15 dB 10 = –12 dB 01 = –9 dB 00 = –6 dB

CODEC PIN DESCRIPTIONS

The ADSP-BF523C/ADSP-BF525C/ADSP-BF527C product adds CODEC signals to those listed in Table 1 of the standard product datasheet ADSP-BF522/523/524/525/526/527 revision PrD.

Table 10. CODEC Pin Descriptions

Pin Name	Type	Function	Pull-Up/Down
CODEC			
CODEC_CLKOUT	O	CODEC Clock Output	None
CODEC_BCLK	I/O	CODEC Digital Audio Bit Clock	Internal Pull-down[1]
DACDAT	I	CODEC Digital Audio Data (DAC) Input	None
DACLRC	I/O	CODEC DAC Sample Rate Left/Right Clock	Internal Pull-down[1]
ADCDAT	O	CODEC ADC Digital Audio Data Output	None
ADCLRC	I/O	CODEC ADC Sample Rate Left/Right Clock	Internal Pull-down[1]
CMODE	I	CODEC Control Interface Selection	Internal Pull-up[1]
CSB	I	CODEC Chip Select Interface Address Selection	Internal Pull-up[1]
CSDA	I/O	CODEC Data Input	None
CSCL	I/O	CODEC Data Clock	None
XTI/ CODEC_MCLK	I	CODEC Crystal Input/ Clock Input	None
XTO	O	CODEC Crystal Output	None
LHPOUT	O	CODEC Left Channel Headphone Output (Analog Output)	None
RHPOUT	O	CODEC Right Channel Headphone Output (Analog Output)	None
LOUT	O	CODEC Left Channel Line Output (Analog Output)	None
ROUT	O	CODEC Right Channel Line Output (Analog Output)	None
VMID	O	CODEC Mid-rail Reference Decoupling Point (Analog Output)	None
MICBIAS	O	CODEC Electret Microphone Bias (Analog Output)	None
MICIN	I	CODEC Microphone Input; (Analog Input, AC Coupled)	None
RLINEIN	I	CODEC Right Channel Line Input (Analog Input, AC Coupled)	None
LLINEIN	I	CODEC Left Channel Line Input (Analog Input, AC Coupled)	None
AVDD	P	CODEC Analog V_{DD}	N/A
AGND	P	CODEC Analog Ground	N/A
HPVDD	P	CODEC Analog Headphone V_{DD}	N/A
HPGND	P	CODEC Headphone Ground	N/A

[1] To conserve power, the pull-up/pull-down is only present when the control register interface is active (= 0).

CODEC OPERATION

This section describes various operating modes for the CODEC.

CODEC RESETTING

The CODEC contains a power-on reset circuit that resets the internal state of the device to a known condition. The power-on reset is applied as V_{DDEXT} powers on and released only after the voltage level of V_{DDEXT} crosses a minimum turn-off threshold. If V_{DDEXT} later falls below a minimum turn-on threshold, the power-on reset is re-applied. The threshold voltages and associated hysteresis are shown in the Electrical Characteristics on Page 32.

The programmer also has the ability to reset the device to a known state using the software control shown in Table 11.

In SPI mode the software reset is applied on the rising edge of CSB and released on the next rising edge of CSCL. In TWI mode the reset is applied for the duration of the ACK signal (approximately one CSCL period) as shown in Figure 27 on Page 25.

Table 11. Software Control of Reset

Register Address	Bit	Label	Default	Description
000 1111	8:0	RESET	Not Reset	Reset Register 00000000 resets the CODEC

Minimizing Pop Noise At The Analog Outputs

Follow these procedures to minimize popping or click noises when the system is powered up or down.

Power Up Sequence

1. Switch on power supplies. By default the CODEC is in standby mode, the DAC is digitally muted, and the audio interface and outputs are all off.
2. Set all required bits in the power down register 6 to '0'; except the OUTPD bit which should be set to '1' (default).
3. Set the required values in all other registers except for the ACTIVE bit in register 9.
4. Set the ACTIVE bit in register 9.
5. The last write of the sequence should set OUTPD to '0' (active) in register 6. This enables the DAC signal path, free of significant power-up noise.

Power Down Sequence

1. Set the OUTPD bit to '1' (power down).
2. Remove the CODEC supplies.

CLOCKING

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronized. This clock is often referred to as the audio system master clock. The CODEC is capable of either generating this system clock or receiving it from an external source.

In applications where the CODEC is the system clock source, a suitable crystal is connected between the XTI/CODEC_MCLK input and XTO output pins as shown in Figure 18.

For applications where the external system generates the reference clock, the external clock can be applied directly through the XTI/CODEC_MCLK input pin. No software configuration is necessary. In this situation, the oscillator circuit of the CODEC can be safely powered down to conserve power (see Power Down Modes on Page 25).

CODEC Clock

The CODEC can be clocked either by CODEC_MCLK or CODEC_MCLK divided by 2. This is controlled by software as shown in Table 12.

Table 12. Software Control of CODEC Clock

Register Address	Bit	Label	Default	Description
000 1000	6	CLKIDIV2	0	CODEC Clock Divider Select 1 = CODEC Clock is CODEC_MCLK ÷ 2 0 = CODEC Clock is CODEC_MCLK

Having a programmable CODEC_MCLK divider allows the device to be used in applications where higher frequency master clocks are available. For example the CODEC can support a master clock of 512 × f_S while operating in a 256 × f_S mode.

Crystal Oscillator

The CODEC includes a crystal oscillator circuit that allows the audio system reference clock to be generated on the CODEC. An external crystal is connected to the CODEC as shown in Figure 18. The crystal oscillator is a low radiation type designed for low EMI.

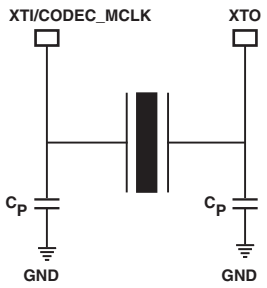

Figure 18. Crystal Connection

The CODEC crystal oscillator provides an extremely low jitter clock. Low jitter clocks are a requirement for high quality audio ADC and DACs. The CODEC architecture is less susceptible than most converter techniques, but still requires clocks with less than approximately 1 ns of jitter. In applications where

there is more than one master clock available, it is recommended that the clock be generated by the CODEC to maximize performance.

CODEC_CLKOUT

The CODEC clock is available to the external audio system on the CODEC_CLKOUT pin. The CODEC clock is buffered for driving external loads. There is no phase inversion between XTI/CODEC_MCLK, the CODEC clock and CODEC_CLKOUT but there will inevitably be some delay. The delay will be dependent on the load that CODEC_CLKOUT drives. See Electrical Characteristics on Page 32.

CODEC_CLKOUT can also be divided by two. See Table 13 for the software control.

CODEC_CLKOUT is disabled and set low whenever the device is in reset.

Table 13. Programming CODEC_CLKOUT

Register Address	Bit	Label	Default	Description
000 1000	7	CLKODIV2	0	CODEC Clock Divider Select 1 = CODEC_CLKOUT is CODEC Clock ÷ 2 0 = CODEC_CLKOUT is CODEC Clock

If CODEC_CLKOUT is not needed, the CODEC_CLKOUT buffer on the CODEC can be safely powered down to conserve power (see Power Down Modes on Page 25). If the programmer has a choice, $f_{CODEC\_CLKOUT} = f_{CODEC\_MCLK}/2$ is recommended to conserve power. CODEC_CLKOUT changes on the rising edge of CODEC_MCLK when $f_{CODEC\_MCLK}/2$ is selected.

DIGITAL AUDIO INTERFACES

The CODEC accommodates four digital audio interface formats.

- Right justified
- Left justified
- I^2S
- Frame Sync mode

These are shown in Figure 19 on Page 17 to Figure 23 on Page 19. See Electrical Characteristics on Page 32 for timing information. These modes operate with 16-bit to 32-bit data except that 32-bit data is not supported in right justified mode. All four of these modes are MSB first.

The digital audio interface takes the data from the internal ADC digital filter and places it on the ADCDAT output. ADCDAT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. ADCLRC is an alignment clock that controls whether left or right channel data is present on the ADCDAT lines. ADCDAT and ADCLRC are synchronous with the CODEC_BCLK signal, with each data bit transition signified by a CODEC_BCLK high-to-low transition. CODEC_BCLK can be an input or an output depending on whether the device is in master or slave mode. See Master and Slave Mode Operation on Page 21.

The digital audio interface also receives the digital audio data for the internal DAC digital filters on the DACDAT input. DACDAT is the formatted digital audio data stream output to the DAC digital filters with left and right channels multiplexed together. DACLRC is an alignment clock that controls whether left or right channel data is present on DACDAT. DACDAT and DACLRC are synchronous with the CODEC_BCLK signal with each data bit transition signified by a CODEC_BCLK high-to-low transition. DACDAT is always an input. CODEC_BCLK and DACLRC are either outputs or inputs depending whether the CODEC is in master or slave mode. See Master and Slave Mode Operation on Page 21.

In all modes DACLRC and ADCLRC must always change on the falling edge of CODEC_BCLK.

Left Justified Mode

Left justified mode is where the MSB is available on the first rising edge of CODEC_BCLK following a ADCLRC or DACLRC transition.

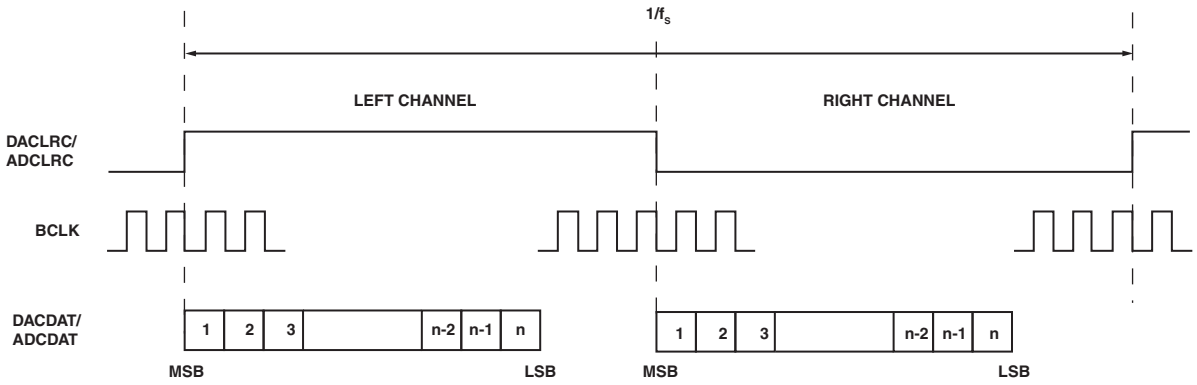

Figure 19. Left Justified Mode

I2S Mode

I^2S mode is where the MSB is available on the second rising edge of CODEC_BCLK following a DACLRC or ADCLRC transition.

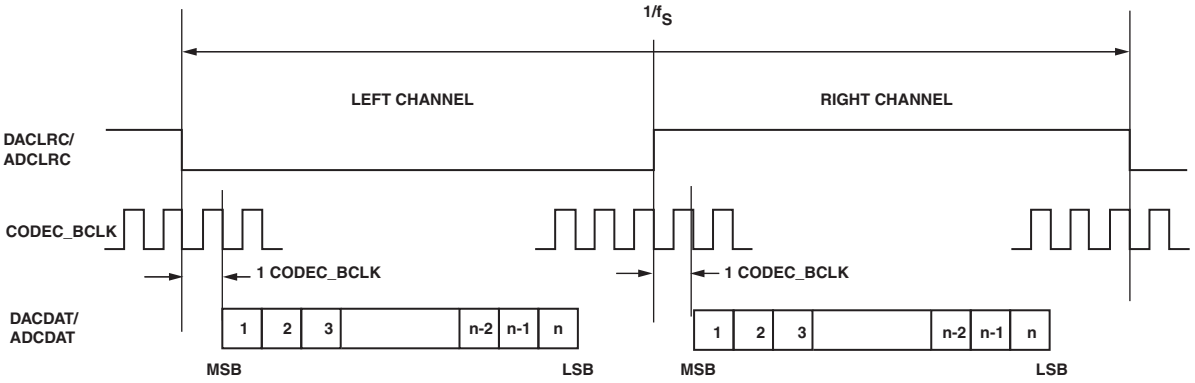

Figure 20. I^2S Mode

Right Justified Mode

Right justified mode is where the LSB is available on the rising edge of CODEC_BCLK preceding a DACLRC or ADCLRC transition, yet MSB is still transmitted first.

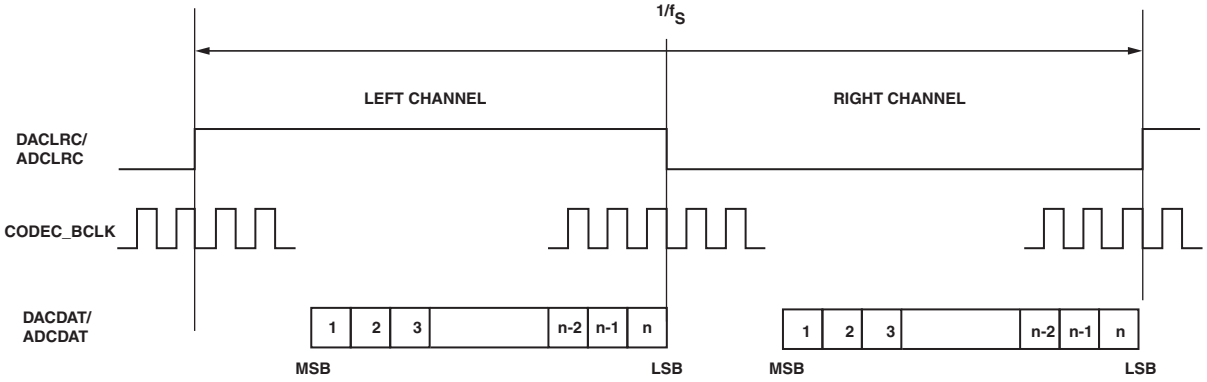

Figure 21. Right Justified Mode

Frame Sync/PCM Mode

In frame sync/PCM mode, the left channel MSB is available on either the first (mode B) or second (mode A) rising edge of CODEC_BCLK (selectable by LRP) following a rising edge of

LRC. Right channel data immediately follows left channel data. Depending on word length, CODEC_BCLK frequency and sample rate—there may be unused CODEC_BCLK cycles between the LSB of the right channel data and the next sample.

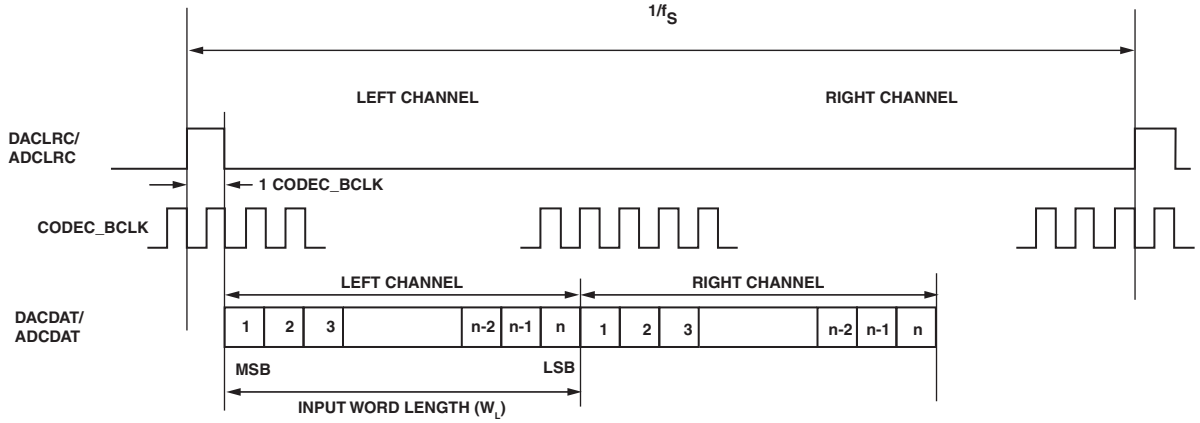

Figure 22. Frame Sync/PCM Mode Audio Interface (Mode A, LRP=1)

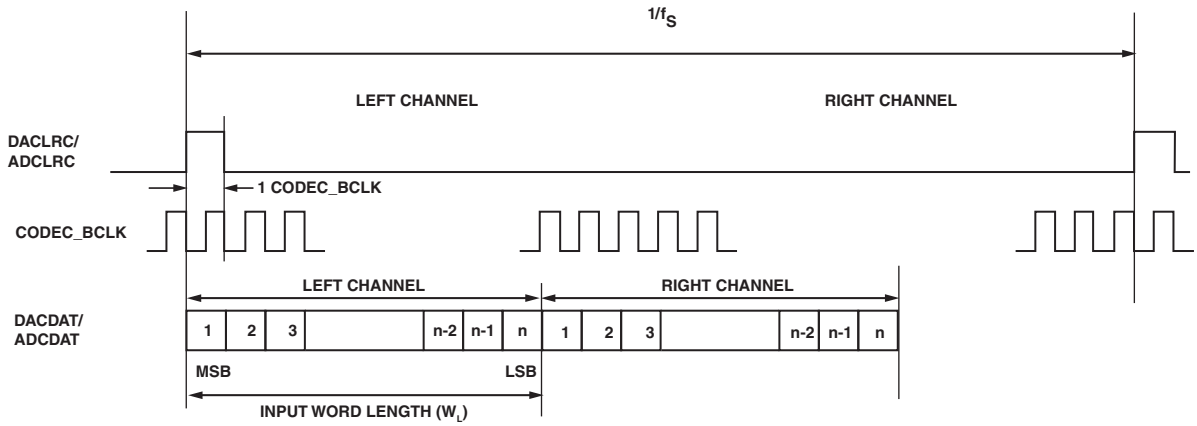

Figure 23. Frame Sync/PCM Mode Audio Interface (Mode B, LRP=0)

Operating the digital audio interface in frame sync mode makes support of the various sample rates and word lengths easier. The only requirement is that all data is transferred within the correct number of CODEC_BCLK cycles to suit the chosen word length.

Mark-Space Ratios

For the digital audio interface to offer similar support in the three other modes (Left Justified, I^2S, and Right Justified), the DACLRC, ADCLRC and CODEC_BCLK frequencies, continuity and mark-space ratios need careful consideration.

In slave mode the DACLRC and ADCLRC inputs are not required to have a 50:50 mark-space ratio. The CODEC_BCLK input need not be continuous. It is however required that there are sufficient CODEC_BCLK cycles for each DACLRC/ADCLRC transition to clock the chosen data word length. The non 50:50 requirement on the LRCs is useful in situations such as a USB 12 MHz clock. Simply dividing down a 12 MHz clock within the processor to generate LRCs and CODEC_BCLK will not generate the appropriate DACLRC or ADCLRC since they will no longer change on the falling edge of CODEC_BCLK. For example, with the 12 MHz/32k×f_S mode there are 375 CODEC_MCLK per LRC. In these situations DACLRC/ADCLRC can be made non 50:50.

In master mode, DACLRC and ADCLRC will be output with a 50:50 mark-space ratio with the CODEC_BCLK output at 64x base frequency (that is, 48 kHz). The exception again is in USB mode where CODEC_BCLK is always 12 MHz. For example in 12 MHz/32k×f_S mode there are 375 master clocks per DACLRC period. Therefore DACLRC and ADCLRC outputs will have a mark space ratio of 187:188.

Mode Configuration

The ADC and DAC digital audio interface modes are software configurable as indicated in Table 14. Dynamically changing the software format may result in erroneous operation of the interfaces and is therefore not recommended.

Table 14. Digital Audio Interface Control

Register Address	Bit	Label	Default	Description
0000111	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = Frame Sync Mode, Frame Sync Plus Two Data Packed Words 10 = I^2S Format, MSB First, Left Justified 01 = MSB First, Left Justified 00 = MSB First, Right Justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32-bits 10 = 24-bits 01 = 20-bits 00 = 16-bits
	4	LRP	0	DACLRC phase control (in left, right or I^2S modes) 1 = Right Channel DAC data when DACLRC high 0 = Right Channel DAC data when DACLRC low (opposite phasing in I^2S mode) or Frame Sync mode A/B select (in Frame Sync mode only) 1 = MSB is available on second CODEC_BCLK rising edge after DACLRC rising edge 0 = MSB is available on first CODEC_BCLK rising edge after DACLRC rising edge
	5	LRSWAP	0	DAC Left Right Clock Swap 1 = Right Channel DAC Data Left 0 = Right Channel DAC Data Right
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	7	BCLKINV	0	Bit Clock Invert 1 = Invert CODEC_BCLK 0 = Do Not Invert CODEC_BCLK

The length of the digital audio data is programmable at 16-, 20-, 24-, or 32-bits in the I^2S or left justified modes only. The data is signed two's complement. Both ADC and DAC are fixed at the same data length. The ADC and DAC digital filters process data using 24-bits. If the ADC is programmed to output 16-bit or 20-bit data then it strips the LSBs from the 24-bit data. If the ADC is programmed to output 32-bits then it packs the LSBs with zeros. If the DAC is programmed to receive 16-bit or 20-bit data, the CODEC packs the LSBs with zeros. If the DAC is programmed to receive 32-bit data, then it strips the LSBs.

The DAC outputs can be swapped under software control using LRP and LRSWAP. Stereo samples are normally generated as a left/right sampled pair. LRSWAP reverses the order so that a left sample goes to the right DAC output and a right sample goes to the left DAC output. LRP swaps the phasing so that a right/left sampled pair is expected and preserves the correct channel phase difference.

To accommodate system timing requirements the interpretation of CODEC_BCLK may be inverted. This is especially appropriate for Frame Sync mode.

ADCDAT lines are always outputs. They power up and return from standby low.

DACDAT is always an input. It is expected to be set low by the audio interface controller when the CODEC is powered off or in standby.

ADCLRC, DACLRC and CODEC_BCLK can be either outputs or inputs depending on whether the CODEC is configured as a master or slave. If the device is a master then the DACLRC and CODEC_BCLK signals are outputs that default low. If the device is a slave then the DACLRC and CODEC_BCLK are inputs. It is expected that these are set low by the audio interface controller when the CODEC is powered off or in standby.

If right justified 32-bit mode is selected then the CODEC defaults to 24-bits.

MASTER AND SLAVE MODE OPERATION

The CODEC can be configured as either a master or slave mode device. As a master mode device the CODEC controls sequencing of the data and clocks on the digital audio interface. As a slave device the CODEC responds with data to the clocks it receives over the digital audio interface. The mode is set with the MS bit of the control register as shown in Table 15.

Table 15. Programming Master/Slave Modes

Register Address	Bit	Label	Default	Description
000 0111	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

As a master mode device the CODEC controls the sequencing of data transfer (ADCDAT, DACDAT) and output of clocks (CODEC_BCLK, ADCLRC, DACLRC) over the digital audio interface. It uses the timing generated from either its on-board crystal or the CODEC_MCLK input as the reference for the clock and data transitions. This is illustrated in Figure 24. ADCDAT is always an output from the CODEC and DACDAT is always an input to the CODEC whether in master or slave mode.

As a slave device the CODEC sequences the data transfer (ADCDAT, DACDAT) over the digital audio interface in response to the external applied clocks (CODEC_BCLK, ADCLRC, DACLRC). This is illustrated in Figure 25.

The CODEC relies on controlled phase relationships between audio interface CODEC_BCLK, DACLRC and the master CODEC_MCLK or CODEC_CLKOUT. To avoid timing hazards, see CODEC Clock Timing on Page 34 for detailed information.

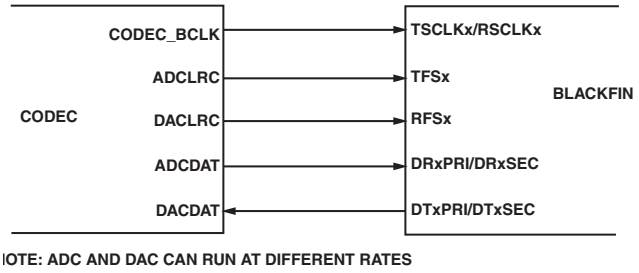

Figure 24. Master Mode

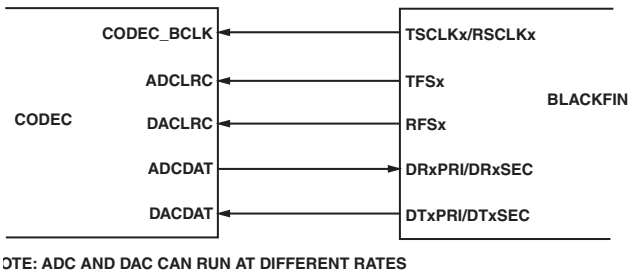

Figure 25. Slave Mode

AUDIO DATA SAMPLING RATES

The CODEC provides for two modes of operation (normal and USB) to generate the required DAC and ADC sampling rates. Use Table 16 to program normal and USB modes.

Table 16. Sample Rate Control

Register Address	Bit	Label	Default	Description
0001000	0	USB/NORMAL	0	Mode Select 1 = USB mode (250/272 × f_S) 0 = Normal mode (256/384 × f_S)
	1	BOSR	0	Base Over-Sampling Rate USB Mode 0 = 250 × f_S 1 = 272 × f_S Normal Mode 96/88.2 kHz 0 = 256 × f_S 0 = 128 × f_S 1 = 384 × f_S 1 = 192 × f_S
	5:2	SR[3:0]	0000	ADC and DAC sample rate control (see Normal Mode Sample Rates and USB Mode Sample Rates on Page 23)

In normal mode, the user controls the sample rate by using an appropriate CODEC_MCLK or crystal frequency and the sample rate control register setting. The CODEC can support sample rates from 8K samples/s up to 96K samples/s.

In USB mode, a fixed CODEC_MCLK or crystal frequency of 12 MHz is used to generate sample rates from 8K samples/s to 96K samples/s. It is called USB mode since the common USB clock is 12 MHz. The CODEC can generate all the normal audio sample rates from this one master clock, without the need for different master clocks or PLL circuits.

The CODEC offers the user the ability to sample the ADC and DAC at different rates under software control in both normal and USB modes. This reduces the burden on a controlling processor. However, signal processing in the ADC and DAC oversampling filters is tightly coupled to minimize power consumption. For that reason, only the combinations of sample rates listed in the following sections are supported. These rates are expected to be the combinations used in typical audio systems.

Normal Mode Sample Rates

In normal mode, the CODEC_MCLK/crystal oscillator is set up according to the desired sample rates of the ADC and DAC. For ADC or DAC sampling rates of 8, 32, 48 or 96 kHz, CODEC_MCLK frequencies of either 12.288 MHz (256 × f_S) or 18.432 MHz (384 × f_S) can be used. For ADC or DAC sampling rates of 8, 44.1 or 88.2 kHz—CODEC_MCLK frequencies of either 11.2896 MHz (256 × f_S) or 16.9344 MHz (384 × f_S) can be used.

Table 17 can be used to set up the device for various sample rate combinations. For example if the user wishes to use the CODEC in normal mode with the ADC and DAC sample rates at 48 kHz

and 48 kHz respectively, then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 for a 12.288 MHz CODEC_MCLK; or with BOSR = 1, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 for a 18.432 MHz CODEC_MCLK. The ADC and DAC will operate with a digital filter of type 1. See Digital Filter Characteristics on Page 39 for an explanation of the different filter types.

The BOSR bit represents the base over-sampling rate. CODEC digital signal processing is carried out at this rate. In normal mode with BOSR = 0, the base over-sampling rate is 256 × f_S. With BOSR = 1, the base over-sampling rate is 384 × f_S. This can be used to determine the actual audio data rate produced by the ADC and required by the DAC.

Table 17. Normal Mode Sample Rate Look-up

Sample Rate (kHz)		CODEC_MCLK Frequency (MHz)	Sample Rate Register Setting[1]					Digital Filter Type
ADC	DAC		BOSR	SR3	SR2	SR1	SR0	
48	48	12.288	0 (256 × f_S)	0	0	0	0	1
		18.432	1 (384 × f_S)	0	0	0	0	1
48	8	12.288	0 (256 × f_S)	0	0	0	1	1
		18.432	1 (384 × f_S)	0	0	0	1	1
8	48	12.288	0 (256 × f_S)	0	0	1	0	1
		18.432	1 (384 × f_S)	0	0	1	0	1
8	8	12.288	0 (256 × f_S)	0	0	1	1	1
		18.432	1 (384 × f_S)	0	0	1	1	1
32	32	12.288	0 (256 × f_S)	0	1	1	0	1
		18.432	1 (384 × f_S)	0	1	1	0	1
96	96	12.288	0 (128 × f_S)	0	1	1	1	2
		18.432	1 (192 × f_S)	0	1	1	1	2
44.1	44.1	11.2896	0 (256 × f_S)	1	0	0	0	1
		16.9344	1 (384 × f_S)	1	0	0	0	1
44.1	8.018	11.2896	0 (256 × f_S)	1	0	0	1	1
		16.9344	1 (384 × f_S)	1	0	0	1	1
8.018	44.1	11.2896	0 (256 × f_S)	1	0	1	0	1
		16.9344	1 (384 × f_S)	1	0	1	0	1
8.018	8.018	11.2896	0 (256 × f_S)	1	0	1	1	1
		16.9344	1 (384 × f_S)	1	0	1	1	1
88.2	88.2	11.2896	0 (128 × f_S)	1	1	1	1	2
		16.9344	1 (192 × f_S)	1	1	1	1	2

[1] Other combinations of BOSR and SR[3:0] are not valid

Examples

1. With ADC data rate 8 kHz, DAC data rate 48 kHz, and CODEC_MCLK = 12.288 MHz—program the device with BOSR = 0 (256 × f_S), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC output data rate will then be exactly 8 kHz (derived from (12.288 MHz/256) x1/6) and the DAC expects data at exactly 48 kHz (derived from 12.288 MHz/256).
2. With ADC data rate 8 kHz, DAC data rate 44.1 kHz, and CODEC_MCLK = 16.9344 MHz— program the device with BOSR = 1 (384 × f_S), SR3 = 1, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will output data at 8.018 kHz ((16.9344 MHz/384) x 2/11) instead of exactly 8.000 kHz. The DAC is still at exactly 44.1 kHz (derived from 16.9344 MHz/384). A slight (sub 0.5%) pitch shift will occur in the 8 kHz audio data and (importantly) the user must ensure that the data across the digital interface is correctly synchronized at the 8.018 kHz rate.

The actual sample rates achieved are shown in Table 18.

Table 18. Normal Mode Actual Sample Rates

Target Sampling Rate	Actual Sampling Rate			
	BOSR = 0		BOSR = 1	
	CODEC_MCLK = 12.288 MHz	CODEC_MCLK = 11.2896 MHz	CODEC_MCLK = 18.432 MHz	CODEC_MCLK = 16.9344 MHz
8 kHz	8 kHz (12.288 MHz/256) × 1/6	8.01 kHz (11.2896 MHz/256) × 2/11	8 kHz (18.432 MHz/384) × 1/6	8.018 kHz (16.9344 MHz/384) × 2/11
32 kHz	32 kHz (12.288 MHz/256) × 2/3	n/a	32 kHz (18.432 MHz/384) × 2/3	n/a
44.1 kHz	n/a	44.1 kHz 11.2896 MHz/256	n/a	44.1 kHz 16.9344 MHz/384
48 kHz	48 kHz 12.288 MHz/256	n/a	48 kHz 18.432 MHz/384	n/a
88.2 kHz	n/a	88.2 kHz (11.2896 MHz/256) × 2	n/a	88.2 kHz (16.9344 MHz/384) × 2
96 kHz	96 kHz (12.288 MHz/256) × 2	n/a	96 kHz (18.432 MHz/384) × 2	n/a

128/192 × fS Normal Mode

The normal mode sample rates are designed for standard 256 × f_S and 384 × f_S CODEC_MCLK rates. The CODEC can also be clocked from a 128 × f_S or 192 × f_S CODEC_MCLK for the limited sampling rates shown in Table 19.

Table 19. 128 × f_S Normal Mode Sample Rate Look-up

Sampling Rate (kHz)		CODEC_MCLK Frequency	Sample Rate Register Setting					Digital Filter Type
ADC	DAC		BOSR	SR3	SR2	SR1	SR0	
48	48	6.144 MHz	0	0	1	1	1	2
		9.216 MHz	1	0	1	1	1	2
44.1	44.1	5.6448 MHz	0	1	1	1	1	2
		8.4672 MHz	1	1	1	1	1	2

512/768×fS Normal Mode

512 × f_S and 768 × f_S CODEC_MCLK rates can be accommodated by using the CLKIDIV2 bit (register 8, bit 6). See Table 16 on Page 21 for software control. The CODEC clock will be divided by two so an external 512/768 × f_S CODEC_MCLK will become 256/384 × f_S internally. The CODEC otherwise operates as in Table 17 on Page 22 but with CODEC_MCLK at twice the specified rate.

USB Mode Sample Rates

In USB mode the CODEC_MCLK/crystal oscillator input is 12 MHz only.

Table 20 can be used to set up the device to work with various sample rate combinations. For example if the ADC and DAC sample rates are 48 kHz and 48 kHz then the CODEC should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0. The ADC and DAC then operate with a digital filter of type 0. See Digital Filter Characteristics on Page 39 for an explanation of the different filter types.

The BOSR bit represents the base over-sampling rate. This is the rate at which the CODEC digital signal processing is carried out. The sampling rate will always be a sub-multiple of the base over-sampling rate. In USB mode, with BOSR = 0, the base over-sampling rate is 250 × f_S. With BOSR = 1, the base over-sampling rate is 272 × f_S. This can be used to determine the actual audio sampling rate produced by the ADC and required by the DAC.

Examples

1. With ADC data sampling rate 8 kHz and DAC data sampling rate 48 kHz—program the device with BOSR = 0 (256 × f_S), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will be exactly 8 kHz ((12 MHz/250) × 1/6) and the DAC expects data at exactly 48 kHz (12 MHz/250).
2. With ADC data rate 8 kHz and DAC data rate 44.1 kHz—program the device with BOSR = 1 (272 × f_S), SR3 = 1, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will output data at 8.021 kHz ((12 MHz/272) × 2/11) instead of exactly 8 kHz and the DAC will be 44.118 kHz (12 MHz/272). A slight (sub 0.5%) pitch shift occurs in the 8 kHz and 44.1 kHz audio data and (importantly) the user must ensure that the data across the digital interface is correctly synchronized at the 8.021 kHz and 44.117 kHz rates.

The actual sample rates achieved are shown in Table 21.

Table 20. USB Mode Sample Rate Look-up

Sampling Rate (kHz)		CODEC_MCLK Frequency (MHz)	Sample Rate Register Setting[1]					Digital Filter Type
ADC	DAC		BOSR	SR3	SR2	SR1	SR0	
48	48	12.000	0	0	0	0	0	0
44.118	44.118	12.000	1	1	0	0	0	1
48	8.021	12.000	0	0	0	0	1	0
44.118	8.021	12.000	1	1	0	0	1	1
8	48	12.000	0	0	0	1	0	0
8.021	44.118	12.000	1	1	0	1	0	1
8	8	12.000	0	0	0	1	1	0
8.021	8.021	12.000	1	1	0	1	1	1
32	32	12.000	0	0	1	1	0	0
96	96	12.000	0	0	1	1	1	3
88.235	88.235	12.000	1	1	1	1	1	2

[1] Other combinations of BOSR and SR[3:0] are not valid

Table 21. USB Mode Actual Sample Rates

Target Sampling Rate	Actual Sampling Rate	
	BOSR = 0 (250 × f_S)	BOSR = 1 (272 × f_S)
8 kHz	8 kHz 12 MHz/(250 x 48/8)	8.021 kHz 12 MHz/(272 x 11/2)
32 kHz	32 kHz 12 MHz/(250 x 48/32)	n/a
44.1 kHz	n/a	44.117 kHz 12 MHz/272
48 kHz	48 kHz 12 MHz/250	n/a
88.2 kHz	n/a	88.235 kHz 12 MHz/136
96 kHz	96 kHz 12 MHz/125	n/a

Activating the Digital Audio Interface

To prevent communication problems, the audio interface is disabled (three-state with a 100 kΩ pulldown) while the interface and sampling control are being programmed. Once programmed, the interface is activated by setting the ACTIVE bit shown in Table 22.

Before changing the digital audio interface or sampling control register the ACTIVE bit should be reset then set.

Table 22. Activating the Audio Interface

Register Address	Bit	Label	Default	Description
000 1001	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive

SOFTWARE CONTROL INTERFACE

Software control can use either a 3-wire (SPI-compatible) or 2-wire (TWI) interface. The interface is selected by setting the CMODE pin shown in Table 23.

Table 23. Control Interface CMode Selection

CMODE	Interface format
0	TWI
1	SPI

In SPI mode, CSDA is used for serial data and CSCL is used for the serial clock. In TWI mode, the state of the CSB pin allows the programmer to select one of two addresses.

SPI Mode

The CODEC can be controlled using an SPI serial interface. CSDA is used for the program data, CSCL is used to clock in the program data and CSB is used to latch the program data. The SPI interface protocol is shown in Figure 26.

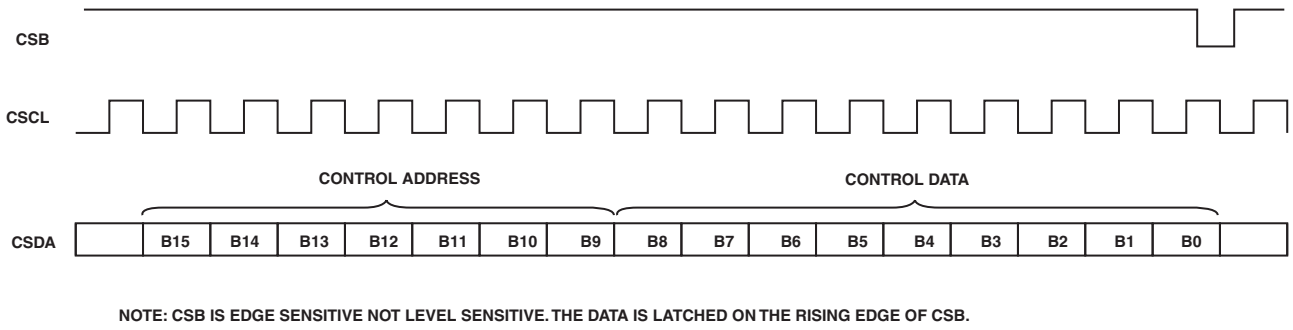

Figure 26. SPI Interface

TWI Mode

The CODEC can be controlled using a 2-wire TWI serial interface. CSDA is used for serial data and CSCL is used for the serial clock. The device operates as a slave device only. The CODEC has one of two slave addresses that are selected by setting the state of pin 15, (CSB). The TWI interface protocol is shown in Figure 26.

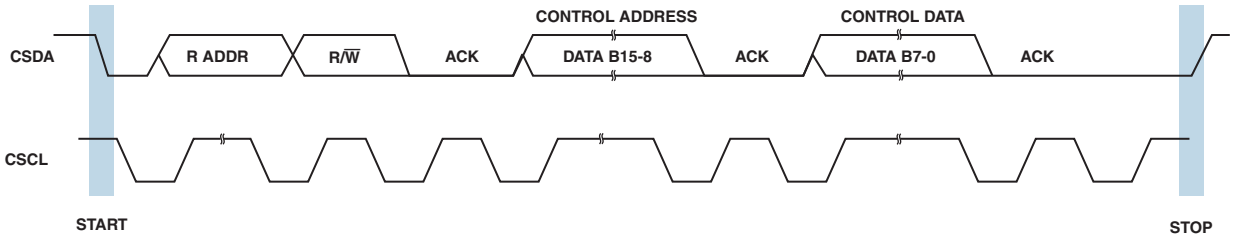

Figure 27. TWI Interface

To control the CODEC using the TWI bus, the master control device initiates a data transfer by establishing a start condition. This is defined by a high-to-low transition on CSDA while CSCL remains high, which indicates that an address and data transfer will follow. All peripherals on the TWI bus respond to the start condition and shift in the next eight bits (7-bit address plus read/write bit). The transfer is MSB first. The 7-bit address consists of a 6-bit base address plus a single programmable bit to select one of two available addresses for this device (see Table 24 on Page 25). If the correct address is received and the read/write bit is '0', indicating a write, the CODEC responds by pulling CSDA low on the next clock pulse (ACK). The CODEC is a write only device and will only respond when the read/write bit indicates a write. If the address is not recognized, the CODEC returns to the idle condition and waits for a new start condition and valid address.

Table 24. TWI Address Selection

CSB State	Address
0	0011010
1	0011011

Once the CODEC has acknowledged a correct address, the controller sends eight data bits ([B15:B8]). The CODEC then acknowledges the data by pulling CSDA low for one clock pulse. The controller then sends the remaining eight data bits ([B7:B0]) and the CODEC then acknowledges again by pulling CSDA low.

A stop condition is defined when there is a low-to-high transition on CSDA while CSCL is high. If a start or stop condition is detected out of sequence at any point in the data transfer then the device jumps to the idle state.

After receiving a complete address and data sequence the CODEC returns to the idle state and waits for another start condition. Each write to a register requires the complete sequence of start condition, device address, and read/write bit followed by the 16-bit register address and data.

POWER DOWN MODES

The CODEC contains power conservation modes where various circuit blocks may be safely powered down. These modes are software programmable as shown in Table 25.

Table 25. Power Conservation Mode Control

Register Address	Bit	Label	Default	Description
000 0110	0	LINEINPD	1	Line Input Power Down 1 = Enable Power Down 0 = Disable Power Down
	1	MICPD	1	Microphone Input and Bias Power Down 1 = Enable Power Down 0 = Disable Power Down
	2	ADCPD	1	ADC Power Down 1 = Enable Power Down 0 = Disable Power Down
	3	DACPD	1	DAC Power Down 1 = Enable Power Down 0 = Disable Power Down
	4	OUTPD	1	Line Output Power Down 1 = Enable Power Down 0 = Disable Power Down
	5	OSCPD	0	Oscillator Power Down 1 = Enable Power Down 0 = Disable Power Down
	6	CLKOUTPD	0	CODEC_CLKOUT power down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	Power Off Device 1 = Device Power Off 0 = Device Power On

The power down control can be used to permanently disable functions when not required in certain applications. Or the modes can be used to dynamically power functions up and down depending on the operating mode, for example during playback or record. If dynamic implementations are used, the special instructions in the following sections should be followed.

LINEINPD

Simultaneously powers down both line inputs. This can be done dynamically without audible effects either on the ADC or on the line outputs in bypass mode. This is useful when the device enters playback, pause or stop modes or when the microphone input is selected.

MICPD

Simultaneously powers down both the microphone input and the microphone bias. If this is done dynamically audible pops through the ADC will result, but they will only be audible if the microphone input is selected to the ADC at the time. If the state of MICPD is changed, the controlling processor should switch the line inputs to the ADC (INSEL) before changing MICPD. This is useful when the device enters playback, pause or stop modes or when the microphone input is not selected.

ADCPD

Powers down the ADC and ADC filters. If this is done dynamically audible pops will result if any signals were passing through the ADC. To avoid popping when the ADC is to be powered down, either mute the microphone input (MUTEIN) or mute the MUTELINEIN, then change ADCPD. This is useful when the device enters playback, pause or stop modes regardless whether microphone or line inputs are selected.

DACPD

Powers down the DAC and DAC digital filters. If this is done dynamically audible pops will result. To prevent pop—the DAC should first be soft-muted (DACMU), then the output should be de-selected from the line and headphone output (DACSEL), and then the DAC powered down (DACPD). This is useful when the device enters record, pause, stop or bypass modes.

OUTPD

Powers down the line and headphone outputs. If this is done dynamically audible pops may result unless the DAC is first soft-muted (DACMU). This is useful when the device enters record, pause or stop modes.

OSCPD

Powers off the on board crystal oscillator. The CODEC_MCLK input functions independently of the oscillator being powered down.

CLKOUTPD

Powers down the CODEC_CLKOUT pin. This conserves power and reduces digital noise and RF emissions. CODEC_CLKOUT is tied low when powered down.

Standby Mode

The device can be put into a standby mode by powering down all the audio circuitry using the software control shown in Table 26. If the crystal oscillator and/or CODEC_CLKOUT pins are being used to derive the master clock, the crystal oscillator can be powered off without powering off CODEC_CLKOUT.

Table 26. Standby Mode

POWER OFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	Description
0	0	0	1	1	1	1	1	STANDBY, with Crystal Oscillator and CODEC_CLKOUT available
0	1	0	1	1	1	1	1	STANDBY, with Crystal Oscillator available, CODEC_CLKOUT not available
0	1	1	1	1	1	1	1	STANDBY, Crystal Oscillator and CODEC_CLKOUT not available.

In standby mode the control interface, and a small portion of the digital and areas of the analog circuitry remain active. The active analog includes the analog VMID reference so that the analog line inputs, line outputs and headphone outputs remain biased to VMID. This reduces audible effects from dc glitches when entering or leaving standby mode.

Power Off Mode

The device can be powered off by writing to the POWEROFF bit of the power down register. In the power off mode, the control interface and a small portion of the digital circuits remain active. The analog VMID reference is disabled. As in standby mode, the crystal oscillator and/or CODEC_CLKOUT pin can be independently controlled. See Table 27.

Table 27. Poweroff Mode

POWER OFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	Description
1	0	0	X	X	X	X	X	POWEROFF, with Crystal Oscillator and CODEC_CLKOUT available
1	1	0	X	X	X	X	X	POWEROFF, with Crystal Oscillator available, CODEC_CLKOUT not available
1	1	1	X	X	X	X	X	POWEROFF, Crystal Oscillator and CODEC_CLKOUT not available

REGISTER MAP

The complete register map is shown in Table 28. The detailed description can be found in Table 29 on Page 27 and in the relevant text of the device description. There are 11 registers with 16-bits per register (7-bit address plus nine bits of data). These can be controlled using either the two wire USB or three wire SPI interface.

Table 28. Program Register Mapping

Register	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	Address							Data								
R0	0	0	0	0	0	0	0	LRINBOTH	LINMUTE	0	0	LINVOL				
R1	0	0	0	0	0	0	1	RLINBOTH	RINMUTE	0	0	RINVOL				
R2	0	0	0	0	0	1	0	LRHPBOTH	LZCEN	LHPVOL						
R3	0	0	0	0	0	1	1	RLHPBOTH	RZCEN	RHPVOL						
R4	0	0	0	0	1	0	0	0	SIDEATT		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST
R5	0	0	0	0	1	0	1	0	0	0	0	HPOR	DACMU	DEEMPH		ADC HPD
R6	0	0	0	0	1	1	0	0	PWROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD
R7	0	0	0	0	1	1	1	0	CODEC_BCLKINV	MS	LRSWAP	LRP	IWL		FORMAT	
R8	0	0	0	1	0	0	0	0	CLKODIV2	CLKIDIV2	SR				BOSR	USB/NORM
R9	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	ACTIVE
R15	0	0	0	1	1	1	1	RESET								

Table 29. Register Descriptions

Register Address	Bit	Label	Default	Description
Register 0 000 0000 Left Line In	4:0	LINVOL[4:0]	10111 (0 dB)	Left Channel Line Input Volume Control 11111 = +12 dB in 1.5 dB steps down to 00000 = –34.5 dB
	7	LINMUTE	1	Left Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[4:0] and LINMUTE to RINVOL[4:0] and RINMUTE 0 = Disable Simultaneous Load
Register 1 000 0001 Right Line In	4:0	RINVOL[4:0]	10111 (0 dB)	Right Channel Line Input Volume Control 11111 = +12 dB in 1.5 dB Steps Down to 00000 = –34.5 dB
	7	RINMUTE	1	Right Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[4:0] and RINMUTE to LINVOL[4:0] and LINMUTE 0 = Disable Simultaneous Load
Register 2 000 0010 Left Headphone Out	6:0	LHPVOL [6:0]	1111001 (0 dB)	Left Channel Headphone Output Volume Control 1111111 = +6 dB in 1 dB Steps Down to 0110000 = –73 dB 0000000 to 0101111 = MUTE
	7	LZCEN	0	Left Channel Zero Cross Detect Enable 1 = Enable 0 = Disable
	8	LRHPBOTH	0	Left to Right Channel Headphone Volume, Mute and Zero Cross Data Load Control 1 = Enable Simultaneous Load of LHPVOL[6:0] and LZCEN to RHPVOL[6:0] and RZCEN 0 = Disable Simultaneous Load

Table 29. Register Descriptions (Continued)

Register Address	Bit	Label	Default	Description
Register 3 000 0011 Right Headphone Out	6:0	RHPVOL [6:0]	1111001 (0 dB)	Right Channel Headphone Output Volume Control 1111111 = +6 dB in 1 dB Steps Down to 0110000 = –73 dB 0000000 to 0101111 = MUTE
	7	RZCEN	0	Right Channel Zero Cross Detect Enable 1 = Enable 0 = Disable
	8	RLHPBOTH	0	Right to Left Channel Headphone Volume, Mute and Zero Cross Data Load Control 1 = Enable Simultaneous Load of RHPVOL[6:0] and RZCEN to LHPVOL[6:0] and LZCEN 0 = Disable Simultaneous Load
Register 4 000 0100 Analog Audio Path Control	0	MICBOOST	0	Microphone Input Level Boost 1 = Enable Boost 0 = Disable Boost
	1	MUTEMIC	1	Mic Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	2	INSEL	0	Microphone/Line Input Select to ADC 1 = Microphone Input Select to ADC 0 = Line Input Select to ADC
	3	BYPASS	1	Bypass Switch 1 = Enable Bypass 0 = Disable Bypass
	4	DACSEL	0	DAC Select 1 = Select DAC 0 = Do Not Select DAC
	5	SIDETONE	0	Side Tone Switch 1 = Enable Side Tone 0 = Disable Side Tone
	7:6	SIDEATT[1:0]	00	Side Tone Attenuation 11 = –15 dB 10 = –12 dB 01 = –9 dB 00 = –6 dB
Register 5 000 0101 Digital Audio Path Control	0	ADCHPD	0	ADC High Pass Filter Enable 1 = Disable High Pass Filter 0 = Enable High Pass Filter
	2:1	DEEMP[1:0]	00	De-emphasis Control 11 = 48 kHz 10 = 44.1 kHz 01 = 32 kHz 00 = Disable
	3	DACMU	1	DAC Soft Mute Control 1 = Enable Soft Mute 0 = Disable Soft Mute
	4	HPOR	0	Store DC Offset When High Pass Filter Disabled 1 = Store Offset 0 = Clear Offset

Table 29. Register Descriptions (Continued)

Register Address	Bit	Label	Default	Description
Register 6 000 0110 Power Down Control	0	LINEINPD	1	Line Input Power Down 1 = Enable Power Down 0 = Disable Power Down
	1	MICPD	1	Microphone Input and Bias Power Down 1 = Enable Power Down 0 = Disable Power Down
	2	ADCPD	1	ADC Power Down 1 = Enable Power Down 0 = Disable Power Down
	3	DACPD	1	DAC Power Down 1 = Enable Power Down 0 = Disable Power Down
	4	OUTPD	1	Outputs Power Down 1 = Enable Power Down 0 = Disable Power Down
	5	OSCPD	0	Oscillator Power Down 1 = Enable Power Down 0 = Disable Power Down
	6	CLKOUTPD	0	CODEC_CLKOUT Power down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	POWEROFF mode 1 = Enable POWEROFF 0 = Disable POWEROFF
Register 7 000 0111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = Frame Sync Mode, Frame Sync Plus Two Data Packed Words 10 = I^2S Format, MSB-First Left–1 Justified 01 = MSB-First, Left Justified 00 = MSB-First, Right Justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32-bits 10 = 24-bits 01 = 20-bits 00 = 16-bits
	4	LRP	0	DACLRC Phase Control (in Left, Right or I^2S Modes) 1 = Right Channel DAC Data When DACLRC High 0 = Right Channel DAC Data When DACLRC Low (Opposite Phasing in I^2S Mode) or Frame Sync Mode A/B Select (in Frame Sync Mode Only) 1 = MSB is Available on Second CODEC_BCLK Rising Edge After DACLRC Rising Edge 0 = MSB is Available on First CODEC_BCLK Rising Edge After DACLRC Rising Edge
	5	LRSWAP	0	DAC Left Right Clock Swap 1 = Right Channel DAC Data Left 0 = Right Channel DAC Data Right
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	7	BCLKINV	0	Bit Clock Invert 1 = Invert CODEC_BCLK 0 = Do Not Invert CODEC_BCLK

Table 29. Register Descriptions (Continued)

Register Address	Bit	Label	Default	Description
Register 8 000 1000 Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB Mode (250/272 × f_S) 0 = Normal Mode (256/384 × f_S)
	1	BOSR	0	Base Over-Sampling Rate USB Mode 0 = 250 × f_S 1 = 272 × f_S Normal Mode 0 = 256 × f_S 1 = 384 × f_S
	5:2	SR[3:0]	0000	ADC and DAC Sample Rate Control; See USB Mode and Normal Mode Sample Rate Sections for Operation
	6	CLKIDIV2	0	CODEC Clock Divider Select 1 = CODEC Clock is CODEC_MCLK Divided by Two 0 = CODEC Clock is CODEC_MCLK
	7	CLKODIV2	0	CODEC_CLKOUT Divider Select 1 = CODEC_CLKOUT is CODEC Clock Divided by Two 0 = CODEC_CLKOUT is CODEC Clock
Register 9 000 1001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive
Register 10 000 1111 Reset Register	8:0	RESET	not reset	Reset Register Writing 0000 0000 to Register Resets Device

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Typical	Max	Unit
AVDD	Analog V_{DD}		1.8		3.6	V
HPVDD	Headphone V_{DD} (Analog)		1.8		3.6	V
V_{ILC}	CODEC Low Level Input Voltage[1]				$0.3 \times V_{DDEXT}$	V
V_{IHC}	CODEC High Level Input Voltage[1]		$0.7 \times V_{DDEXT}$			V
V_{OLC}	CODEC Low Level Output Voltage[1]				$0.1 \times V_{DDEXT}$	V
V_{OHC}	CODEC Low Level Output Voltage[1]		$0.9 \times V_{DDEXT}$			V

[1] Parameter value applies to digital signal pins (ADCDAT, ADCLRC, CODEC_BCLK, CSB, CODEC_CLKOUT, CMODE, DACDAT, DACLRC, CSCL, CSDA, XTI/CODEC_MCLK, XTO).

POWER CONSUMPTION

Table 30. Powerdown Mode Current Consumption

Mode Description	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	Current Consumption[1, 2, 3, 4, 5] Typical AVDD (1.8V)	HPVDD (1.8V)	V_{DDEXT} (1.8V)	Unit
Record and Playback												
All active, Oscillator Enabled	0	0	0	0	0	0	0	0	6	0.6	0.9	mA
Playback Only												
Oscillator Enabled	0	0	0	0	0	1	1	1	1.7	0.6	0.9	mA
Record Only												
Line Record, Oscillator Enabled	0	0	0	1	1	0	1	0	3.9		0.9	mA
Mic Record, Oscillator Enabled	0	0	0	1	1	0	0	1	3.6		0.9	mA
Side Tone (Microphone Input to Headphone Output)												
Clock Stopped	0	0	1	0	1	1	0	1	0.8	0.6		mA
Analog Bypass (Line-in to Line-out)												
Clock Stopped	0	0	1	0	1	1	1	0	1.1	0.6		mA
Standby												
Clock Stopped	0	1	1	1	1	1	1	1	8			µA
Power Down												
Clock Stopped	1	1	1	1	1	1	1	1	0.2	0.2	0.2	µA

[1] These current consumption values are for the CODEC alone. Please refer to the published ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 Revision PrD datasheet for the additional current consumption of the Blackfin processor.

[2] AVDD, HPVDD, V_{DDEXT} = 1.8V, AGND = 0V, T_A = +25°C. Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S (12.288 MHz).

[3] All values are quiescent, with no signal.

[4] All values are measured with the audio interface in master mode (MS = 1).

[5] The power dissipation in the headphone itself is not included in this table.

ELECTRICAL CHARACTERISTICS

Parameter[1]		Conditions[2]	Min	Typical	Max	Unit
Line Input to ADC						
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ f_S = 48 kHz	tbd	85		dB
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ f_S = 96 kHz		85		dB
DR	Dynamic Range	A-weighted, –60 dB Full Scale Input	tbd	88		dB
THD	Total Harmonic Distortion	–1 dB Input, 0 dB Gain		–76	tbd	dB
Microphone Input to ADC		0 dB Gain, f_S = 48 kHz, 40 kΩ Source Impedance				
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain		80		dB
DR	Dynamic Range	A-weighted, –60 dB Full Scale Input		70		dB
THD	Total Harmonic Distortion	0 dB Input, 0 dB Gain		–55		dB
Line Output for DAC Playback Only		Load = 10 kΩ, 50 pF				
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ f_S = 48 kHz	tbd	95		dB
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ f_S = 96 kHz		93		dB
DR	Dynamic Range	A-weighted, –60 dB Full Scale Input	tbd	90		dB
THD	Total Harmonic Distortion	1 kHz, 0 dB		–80	tbd	dB
THD	Total Harmonic Distortion	1 kHz, –3 dB		–90		dB
Analog Line Input to Line Output		Load = 10 k Ω, 50 pF, No Gain on Input, Bypass Mode				
SNR	Signal to Noise Ratio		tbd	90		dB
THD	Total Harmonic Distortion	1 kHz, 0 dB		–83	tbd	dB
THD	Total Harmonic Distortion	1 kHz, –3 dB		–92		dB
Stereo Headphone Output						
PO	Maximum Output Power	R_L = 32 Ω		9		mW
PO	Maximum Output Power	R_L = 16 Ω		18		mW
SNR	Signal to Noise Ratio	A-weighted	tbd	95		dB
THD	Total Harmonic Distortion	1 kHz, –5 dB, R_L = 32 Ω, Full Scale Input		–62	tbd	dB
THD	Total Harmonic Distortion	1 kHz,–2 dB, R_L = 32 Ω, Full Scale Input			tbd	dB
Microphone Input to Headphone Output Side Tone Mode						
SNR	Signal to Noise Ratio		tbd	90		dB

[1] SNR is the ratio of output level with 1 kHz full scale input, to the output level with the input short-circuited, measured 'A' weighted over a 20Hz to 20 kHz bandwidth using an audio analyzer. Ratio of output level with 1 kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20 Hz to 20 kHz bandwidth. All performance measurements are done with a 20 kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in these specifications. The low pass filter removes out of band noise; which is not audible but may affect dynamic specification values. VMID is decoupled with 10 µF and 0.1 µF capacitors (smaller values may result in reduced performance).

[2] AVDD, HPVDD, V_{DDEXT} = 1.8V, AGND = 0V, T_A = +25°C. Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S (12.288 MHz) unless otherwise stated.

Signal-to-noise ratio (SNR) (dB) is a measure of the difference in level between the full scale output and the output with no signal applied.

Dynamic range (DR) (dB) is a measure of the difference between the highest and lowest portions of a signal, normally a THD+N measurement at 60 dB below full scale. The measured signal is then corrected by adding the 60 dB to it. For example THD+N @ –60 dB = –32 dB, DR = 92 dB.

Total Harmonic Distortion Plus Noise (THD+N) (dB) is a ratio of the rms values of (Noise + Distortion)/Signal.

Channel Separation (dB)—Also known as crosstalk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

PACKAGE INFORMATION

The information presented in Figure 28 and Table 31 provides details about the package branding for the ADSP-BF523C/ADSP-BF525C/ADSP-BF527C processor. For a complete listing of product availability, see Ordering Guide on Page 44.

Figure 28. Product Information on Package

Table 31. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

CODEC CLOCK TIMING

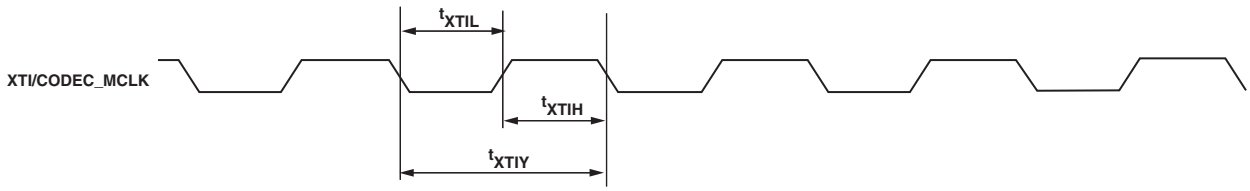

Figure 29. CODEC Clock Timing Requirements

Table 32. CODEC Clock Timing Requirements

Parameter		Test Conditions[1]	Min	Typical	Max	Unit
t_{XTIH}	XTI/CODEC_MCLK System clock pulse width high		18			ns
t_{XTIL}	XTI/CODEC_MCLK System clock pulse width low		18			ns
t_{XTIY}	XTI/CODEC_MCLK System clock cycle time		54			ns
	XTI/CODEC_MCLK Duty cycle		40:60		60:40	

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode f_s = 48 kHz, XTI/CODEC_MCLK = 256 × f_s unless otherwise stated.

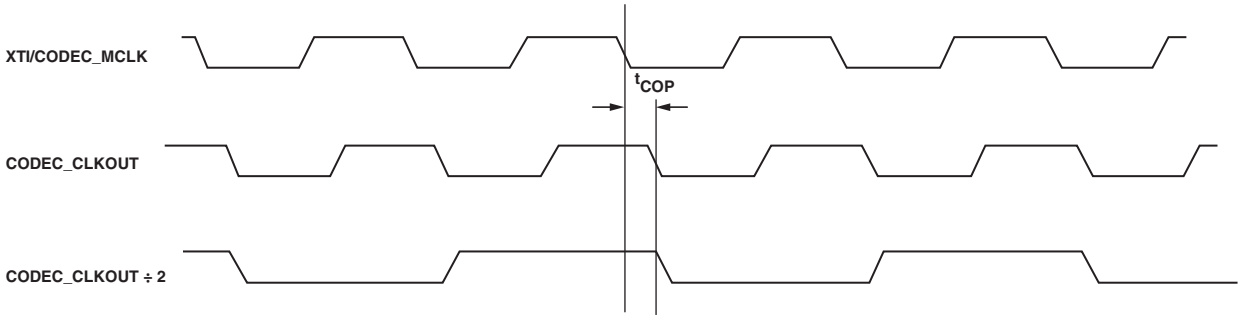

Figure 30. CODEC_CLKOUT Timing Requirements

Table 33. Clock Out Timing Requirements

Parameter		Test Conditions[1]	Min	Typical	Max	Unit
t_{COP}	CODEC_CLKOUT propagation delay from XTI/CODEC_MCLK falling edge		0		10	ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3V, AGND = 0V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

DIGITAL AUDIO INTERFACE—MASTER MODE

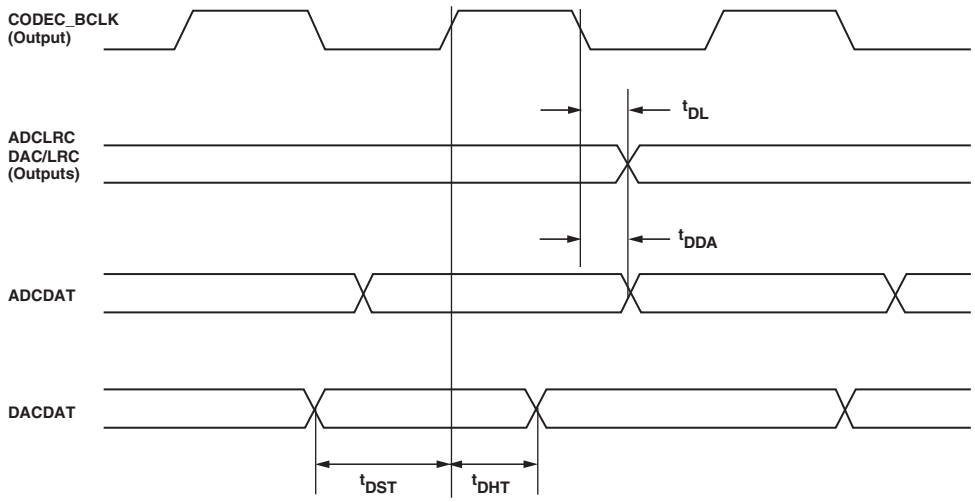

Figure 31. Digital Audio Data Timing—Master Mode

Table 34. Digital Audio Data Timing—Master Mode

Parameter		Test Conditions[1]	Min	Typical	Max	Unit
t_{DL}	ADCLRC/DACLRC propagation delay from CODEC_BCLK falling edge		0		10	ns
t_{DDA}	ADCDAT propagation delay from CODEC_BCLK falling edge		0		15	ns
t_{DST}	DACDAT setup time to CODEC_BCLK rising edge		10			ns
t_{DHT}	DACDAT hold time from CODEC_BCLK rising edge		10			ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

DIGITAL AUDIO INTERFACE—SLAVE MODE

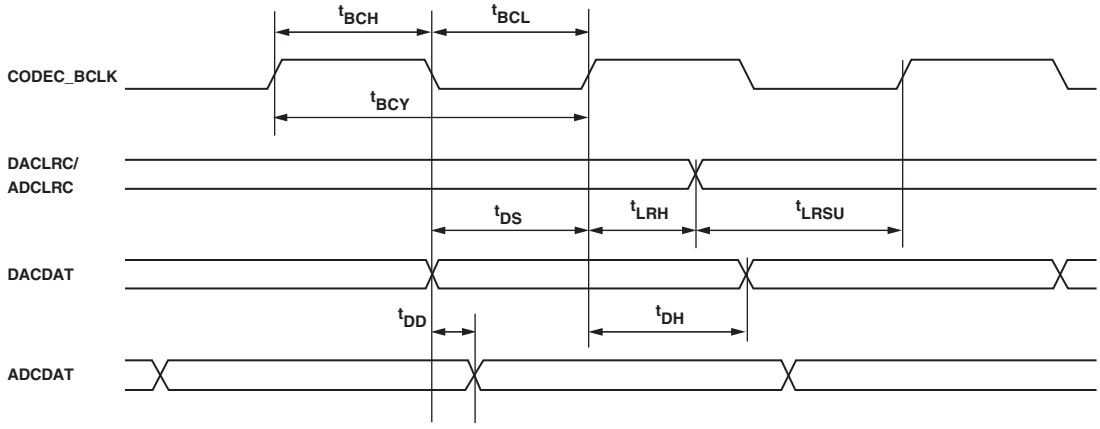

Figure 32. Digital Audio Data Timing—Slave Mode

Table 35. Digital Audio Data Timing—Slave Mode

Parameter		Test Conditions[1]	Min	Typical	Max	Unit
t_{BCY}	CODEC_BCLK cycle time		50			ns
t_{BCH}	CODEC_BCLK pulse width high		20			ns
t_{BCL}	CODEC_BCLK pulse width low		20			ns
t_{LRSU}	DACLRC/ADCLRC set-up time to CODEC_BCLK rising edge		10			ns
t_{LRH}	DACLRC/ADCLRC hold time from CODEC_BCLK rising edge		10			ns
t_{DS}	DACDAT set-up time to CODEC_BCLK rising edge		10			ns
t_{DH}	DACDAT hold time from CODEC_BCLK rising edge		10			ns
t_{DD}	ADCDAT propagation delay from CODEC_BCLK falling edge		0		10	ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

BLACKFIN SPI/TWI INTERFACE TIMING

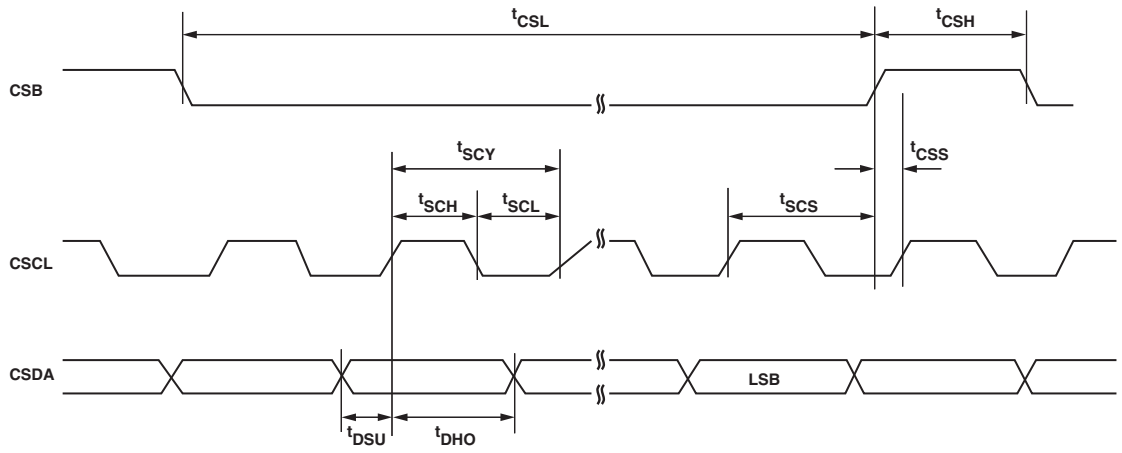

Figure 33. Program Register Input Timing—SPI Serial Control Mode

Table 36. Program Register Input Timing—SPI Serial Control Mode

Parameter		Test Conditions[1]	Min	Typical	Max	Unit
t_{SCS}	CSCL rising edge to CSB rising edge		60			ns
t_{SCY}	CSCL pulse cycle time		80			ns
t_{SCL}	CSCL pulse width low		20			ns
t_{SCH}	CSCL pulse width high		20			ns
t_{DSU}	CSDA to CSCL set-up time		20			ns
t_{DHO}	CSCL to CSDA hold time		20			ns
t_{CSL}	CSB pulse width low		20			ns
t_{CSH}	CSB pulse width high		20			ns
t_{CSS}	CSB rising to CSCL rising		20			ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

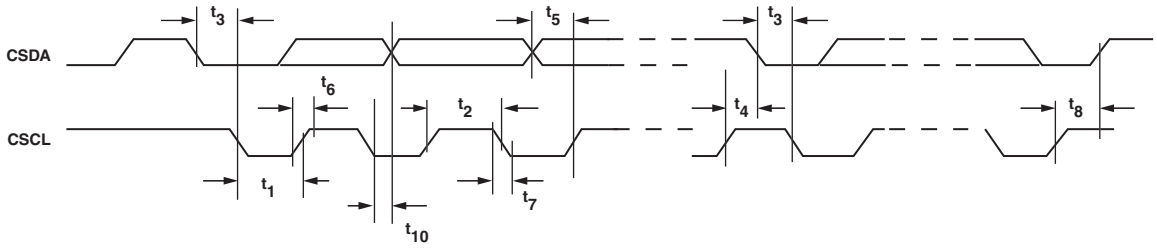

Figure 34. Program Register Input Timing—TWI Serial Control Mode

Table 37. Program Register Input Timing—TWI Serial Control Mode

Parameter		Test Conditions[1]	Min	Typical	Max	Unit
	CSCL Frequency		0		526	kHz
t1	CSCL Low Pulsewidth		1.3			us
t2	CSCL High Pulsewidth		600			ns
t3	Hold Time (Start Condition)		600			ns
t4	Setup Time (Start Condition)		600			ns
t5	Data Setup Time		100			ns
t6	CSDA, CSCL Rise Time				300	ns
t7	CSDA, CSCL Fall Time				300	ns
t8	Setup Time (Stop Condition)		600			ns
t10	Data Hold Time				900	ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

DIGITAL FILTER CHARACTERISTICS

Stop Band Attenuation (dB) is the degree to which the frequency spectrum is attenuated (outside audio band)

Pass-band Ripple is any variation of the frequency response in the pass-band region

The ADC and DAC employ different digital filters. There are four types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in Table 38, the responses of all filters is shown in the proceeding pages.

Table 38. Digital Filter Characteristics

Parameter	Conditions	Min	Typical	Max	Unit
ADC Filter					
Passband	±0.05 dB	tbd × f_S		tbd × f_S	
Passband	–6 dB		0.5 × f_S		
Passband Ripple				tbd	dB
Stopband		tbd × f_S			
Stopband Attenuation	f > 0.5465 × f_S	tbd			dB
High Pass Filter Corner Frequency	–3 dB		3.7		Hz
High Pass Filter Corner Frequency	–0.5 dB		10.4		Hz
High Pass Filter Corner Frequency	–0.1 dB		21.6		Hz
DAC Filter					
Passband	±0.03 dB	tbd × f_S		tbd × f_S	
Passband	–6 dB		0.5 × f_S		
Passband Ripple				tbd	dB
Stopband		tbd × f_S			
Stopband Attenuation	f > 0.5465 × f_S	tbd			dB

Table 39. ADC/DAC Digital Filters Group Delay

Mode	Group Delay	
	DAC Filters	ADC Filters
0	11÷ f_S	12 ÷ f_S
1	18 ÷ f_S	20 ÷ f_S
2	5 ÷ f_S	3 ÷ f_S
3	5 ÷ f_S	6 ÷ f_S

ADC HIGH PASS FILTER

The CODEC has a selectable digital high pass filter to remove dc offsets. The filter response is characterized by the following polynomial.

$$H(z) = (1 - z^{-1})/(1 - 0.9995 \times z^{-1})$$

289-BALL MINI-BGA PINOUT

Table 40 lists the mini-BGA pinout by signal mnemonic.
Table 41 on Page 42 lists the mini-BGA pinout by ball number.

Table 40. 289-Ball Mini-BGA Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{\text{ABE0}}$/SDQM0	AB9	CSB	D23	GND	L14	PF5	B10	$\overline{\text{RESET}}$	V22	VDDEXT	R17	VDDMEM	U8
$\overline{\text{ABE1}}$/SDQM1	AC9	CSCL	B23	GND	L15	PF6	B12	RHPOUT	B21	VDDEXT	T17	VDDMEM	U9
ADCDAT	A16	CSDA	C23	GND	M9	PF7	B13	RLINEIN	F23	VDDEXT	U17	VDDMEM	U10
ADCLRC	A15	DACDAT	A18	GND	M10	PF8	B16	ROUT	G22	VDDINT	B5	VDDMEM	U11
ADDR1	AB8	DACLRC	A17	GND	M11	PF9	A20	RTXI	U23	VDDINT	H8	VDDMEM	U12
ADDR2	AC8	DATA0	Y1	GND	M12	PF10	B15	RTXO	V23	VDDINT	H9	VDDMEM	U13
ADDR3	AB7	DATA1	V2	GND	M13	PF11	B17	SA10	AC10	VDDINT	H10	VDDMEM	U14
ADDR4	AC7	DATA2	W1	GND	M14	PF12	B18	$\overline{\text{SCAS}}$	AC11	VDDINT	H11	VDDMEM	U15
ADDR5	AC6	DATA3	U2	GND	M15	PF13	B19	SCKE	AB13	VDDINT	H12	VDDMEM	U16
ADDR6	AB6	DATA4	V1	GND	N9	PF14	A9	SCL	B22	VDDINT	H13	VDDOTP	AC12
ADDR7	AB4	DATA5	U1	GND	N10	PF15	A10	SDA	C22	VDDINT	H14	VDDRTC	W23
ADDR8	AB5	DATA6	T2	GND	N11	PG0	H2	$\overline{\text{SMS}}$	AC13	VDDINT	H15	VDDUSB	W22
ADDR9	AC5	DATA7	T1	GND	N12	PG1	G1	$\overline{\text{SRAS}}$	AB12	VDDINT	H16	VDDUSB	Y23
ADDR10	AC4	DATA8	R1	GND	N13	PG2	H1	SS/PG	AC20	VDDINT	J8	VMID	G23
ADDR11	AB3	DATA9	P1	GND	N14	PG3	F1	$\overline{\text{SWE}}$	AB10	VDDINT	J16	VROUT	AC18
ADDR12	AC3	DATA10	P2	GND	N15	PG4	D1	TCK	L1	VDDINT	K8	VRSEL	AB22
ADDR13	AB2	DATA11	R2	GND	P9	PG5	D2	TDI	J1	VDDINT	K16	XTAL	P23
ADDR14	AC2	DATA12	N1	GND	P10	PG6	C2	TDO	K1	VDDINT	L8	XTI/CODEC_MCLK	A22
ADDR15	AA2	DATA13	N2	GND	P11	PG7	B1	TMS	L2	VDDINT	L16	XTO	A21
ADDR16	W2	DATA14	M2	GND	P12	PG8	C1	TRST	K2	VDDINT	M8		
ADDR17	Y2	DATA15	M1	GND	P13	PG9	B2	USB_DM	AB21	VDDINT	M16		
ADDR18	AA1	EMU	J2	GND	P14	PG10	B4	USB_DP	AA22	VDDINT	N8		
ADDR19	AB1	EXT_WAKE	AC19	GND	P15	PG11	B3	USB_ID	Y22	VDDINT	N16		
HPGND	G17	GND	A1	GND	R9	PG12	A2	USB_RSET	AC21	VDDINT	P8		
AGND	H22	GND	A23	GND	R10	PG13	A3	USB_VBUS	AB20	VDDINT	P16		
$\overline{\text{AMS0}}$	AC17	GND	B6	GND	R11	PG14	A4	USB_VREF	AC22	VDDINT	R8		
$\overline{\text{AMS1}}$	AB16	GND	J9	GND	R12	PG15	A5	USB_XI	AB23	VDDINT	R16		
$\overline{\text{AMS2}}$	AC16	GND	J10	GND	R13	PH0	A11	USB_XO	AA23	VDDINT	T8		
$\overline{\text{AMS3}}$	AB15	GND	J11	GND	R14	PH1	A12	VDDEXT	G7	VDDINT	T9		
$\overline{\text{AOE}}$	AC15	GND	J12	GND	R15	PH2	A13	VDDEXT	G8	VDDINT	T10		
ARDY	AC14	GND	J13	GND	T22	PH3	B14	VDDEXT	G9	VDDINT	T11		
$\overline{\text{ARE}}$	AB17	GND	J14	GND	AC1	PH4	A14	VDDEXT	G10	VDDINT	T12		
HPVDD	G16	GND	J15	GND	AC23	PH5	K23	VDDEXT	G11	VDDINT	T13		
AVDD	J22	GND	K9	LHPOUT	B20	PH6	K22	VDDEXT	G12	VDDINT	T14		
$\overline{\text{AWE}}$	AB14	GND	K10	LLINEIN	E23	PH7	L23	VDDEXT	G13	VDDINT	T15		
CODEC_BCLK	A19	GND	K11	LOUT	F22	PH8	L22	VDDEXT	G14	VDDINT	T16		
BMODE0	G2	GND	K12	MICBIAS	H23	PH9	T23	VDDEXT	G15	VDDMEM	J7		

Table 40. 289-Ball Mini-BGA Ball Assignment (Alphabetically by Signal) (Continued) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
BMODE1	F2	GND	K13	MICIN	J23	PH10	M22	VDDEXT	H7	VDDMEM	K7		
BMODE2	E1	GND	K14	NMI	U22	PH11	R22	VDDEXT	H17	VDDMEM	L7		
BMODE3	E2	GND	K15	VPPOTP	AB11	PH12	M23	VDDEXT	J17	VDDMEM	M7		
CODEC_CLKOUT	D22	GND	L9	PF0	A7	PH13	N22	VDDEXT	K17	VDDMEM	N7		
CLKBUF	AB19	GND	L10	PF1	B8	PH14	N23	VDDEXT	L17	VDDMEM	P7		
CLKIN	R23	GND	L11	PF2	A8	PH15	P22	VDDEXT	M17	VDDMEM	R7		
CLKOUT	AB18	GND	L12	PF3	B9	PPICLK/TMRCLK	A6	VDDEXT	N17	VDDMEM	T7		
CMODE	E22	GND	L13	PF4	B11	PPIFS1/TMR0	B7	VDDEXT	P17	VDDMEM	U7		

Table 41. 289-Ball Mini-BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	B23	CSCL	H22	AGND	L22	PH8	P22	PH15	U22	NMI	AC5	ADDR9
A2	PG12	C1	PG8	H23	MICBIAS	L23	PH7	P23	XTAL	U23	RTXI	AC6	ADDR5
A3	PG13	C2	PG6	J1	TDI	M1	DATA15	R1	DATA8	V1	DATA4	AC7	ADDR4
A4	PG14	C22	SDA	J2	EMU	M2	DATA14	R2	DATA11	V2	DATA1	AC8	ADDR2
A5	PG15	C23	CSDA	J7	VDDMEM	M7	VDDMEM	R7	VDDMEM	V22	$\overline{\text{RESET}}$	AC9	$\overline{\text{ABE1}}$/SDQM1
A6	PPICLK/TMRCLK	D1	PG4	J8	VDDINT	M8	VDDINT	R8	VDDINT	V23	RTXO	AC10	SA10
A7	PF0	D2	PG5	J9	GND	M9	GND	R9	GND	W1	DATA2	AC11	$\overline{\text{SCAS}}$
A8	PF2	D22	CODEC_CLKOUT	J10	GND	M10	GND	R10	GND	W2	ADDR16	AC12	VDDOTP
A9	PF14	D23	CSB	J11	GND	M11	GND	R11	GND	W22	VDDUSB	AC13	$\overline{\text{SMS}}$
A10	PF15	E1	BMODE2	J12	GND	M12	GND	R12	GND	W23	VDDRTC	AC14	ARDY
A11	PH0	E2	BMODE3	J13	GND	M13	GND	R13	GND	Y1	DATA0	AC15	$\overline{\text{AOE}}$
A12	PH1	E22	CMODE	J14	GND	M14	GND	R14	GND	Y2	ADDR17	AC16	$\overline{\text{AMS2}}$
A13	PH2	E23	LLINEIN	J15	GND	M15	GND	R15	GND	Y22	USB_ID	AC17	$\overline{\text{AMS0}}$
A14	PH4	F1	PG3	J16	VDDINT	M16	VDDINT	R16	VDDINT	Y23	VDDUSB	AC18	VROUT
A15	ADCLRC	F2	BMODE1	J17	VDDEXT	M17	VDDEXT	R17	VDDEXT	AA1	ADDR18	AC19	EXT_WAKE
A16	ADCDAT	F22	LOUT	J22	AVDD	M22	PH10	R22	PH11	AA2	ADDR15	AC20	SS/PG
A17	DACLRC	F23	RLINEIN	J23	MICIN	M23	PH12	R23	CLKIN	AA22	USB_DP	AC21	USB_RSET
A18	DACDAT	G1	PG1	K1	TDO	N1	DATA12	T1	DATA7	AA23	USB_XO	AC22	USB_VREF
A19	CODEC_BCLK	G2	BMODE0	K2	TRST	N2	DATA13	T2	DATA6	AB1	ADDR19	AC23	GND
A20	PF9	G7	VDDEXT	K7	VDDMEM	N7	VDDMEM	T7	VDDMEM	AB2	ADDR13		
A21	XTO	G8	VDDEXT	K8	VDDINT	N8	VDDINT	T8	VDDINT	AB3	ADDR11		
A22	XTI/CODEC_MCLK	G9	VDDEXT	K9	GND	N9	GND	T9	VDDINT	AB4	ADDR7		
A23	GND	G10	VDDEXT	K10	GND	N10	GND	T10	VDDINT	AB5	ADDR8		
B1	PG7	G11	VDDEXT	K11	GND	N11	GND	T11	VDDINT	AB6	ADDR6		
B2	PG9	G12	VDDEXT	K12	GND	N12	GND	T12	VDDINT	AB7	ADDR3		
B3	PG11	G13	VDDEXT	K13	GND	N13	GND	T13	VDDINT	AB8	ADDR1		
B4	PG10	G14	VDDEXT	K14	GND	N14	GND	T14	VDDINT	AB9	$\overline{\text{ABE0}}$/SDQM0		
B5	VDDINT	G15	VDDEXT	K15	GND	N15	GND	T15	VDDINT	AB10	$\overline{\text{SWE}}$		
B6	GND	G16	HPVDD	K16	VDDINT	N16	VDDINT	T16	VDDINT	AB11	VPPOTP		
B7	PPIFS1/TMR0	G17	HPGND	K17	VDDEXT	N17	VDDEXT	T17	VDDEXT	AB12	$\overline{\text{SRAS}}$		
B8	PF1	G22	ROUT	K22	PH6	N22	PH13	T22	GND	AB13	SCKE		
B9	PF3	G23	VMID	K23	PH5	N23	PH14	T23	PH9	AB14	$\overline{\text{AWE}}$		
B10	PF5	H1	PG2	L1	TCK	P1	DATA9	U1	DATA5	AB15	$\overline{\text{AMS3}}$		
B11	PF4	H2	PG0	L2	TMS	P2	DATA10	U2	DATA3	AB16	$\overline{\text{AMS1}}$		
B12	PF6	H7	VDDEXT	L7	VDDMEM	P7	VDDMEM	U7	VDDMEM	AB17	$\overline{\text{ARE}}$		
B13	PF7	H8	VDDINT	L8	VDDINT	P8	VDDINT	U8	VDDMEM	AB18	CLKOUT		
B14	PH3	H9	VDDINT	L9	GND	P9	GND	U9	VDDMEM	AB19	CLKBUF		
B15	PF10	H10	VDDINT	L10	GND	P10	GND	U10	VDDMEM	AB20	USB_VBUS		
B16	PF8	H11	VDDINT	L11	GND	P11	GND	U11	VDDMEM	AB21	USB_DM		
B17	PF11	H12	VDDINT	L12	GND	P12	GND	U12	VDDMEM	AB22	VRSEL		

Table 41. 289-Ball Mini-BGA Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
B18	PF12	H13	VDDINT	L13	GND	P13	GND	U13	VDDMEM	AB23	USB_XI		
B19	PF13	H14	VDDINT	L14	GND	P14	GND	U14	VDDMEM	AC1	GND		
B20	LHPOUT	H15	VDDINT	L15	GND	P15	GND	U15	VDDMEM	AC2	ADDR14		
B21	RHPOUT	H16	VDDINT	L16	VDDINT	P16	VDDINT	U16	VDDMEM	AC3	ADDR12		
B22	SCL	H17	VDDEXT	L17	VDDEXT	P17	VDDEXT	U17	VDDEXT	AC4	ADDR10		

Figure 36 shows the top view of the mini-BGA ball configuration. Figure 35 shows the bottom view of the mini-BGA ball configuration.

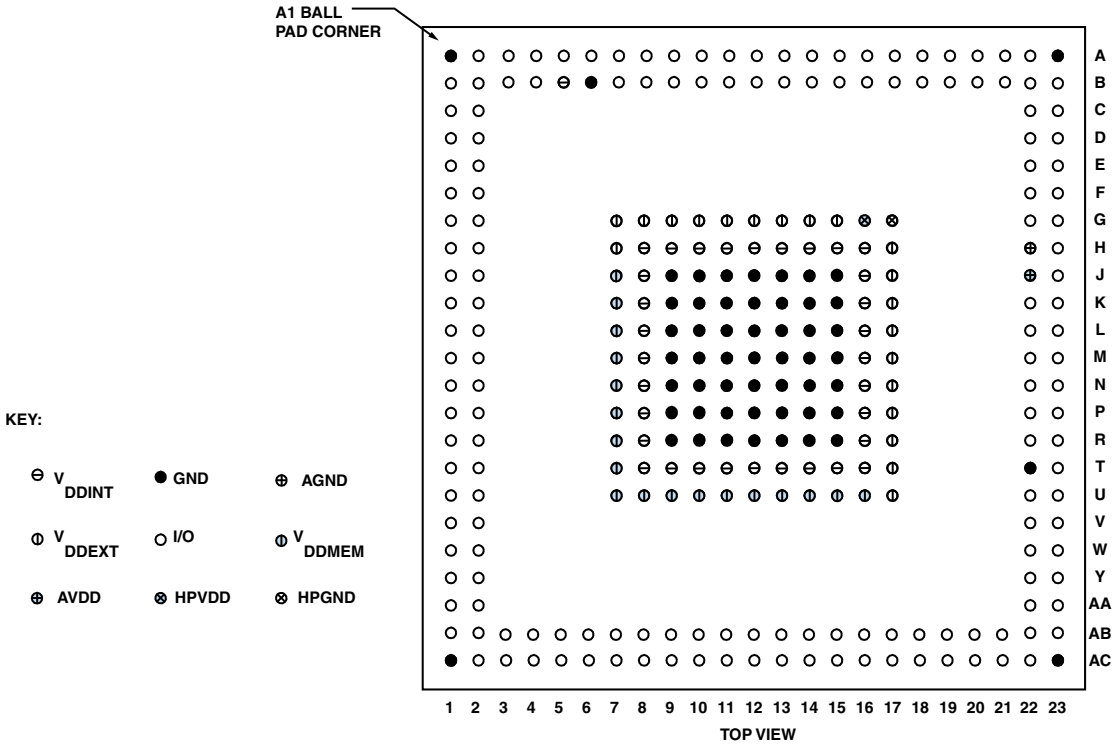

Figure 35. 289-Ball Mini-BGA Ball Configuration (Top View)

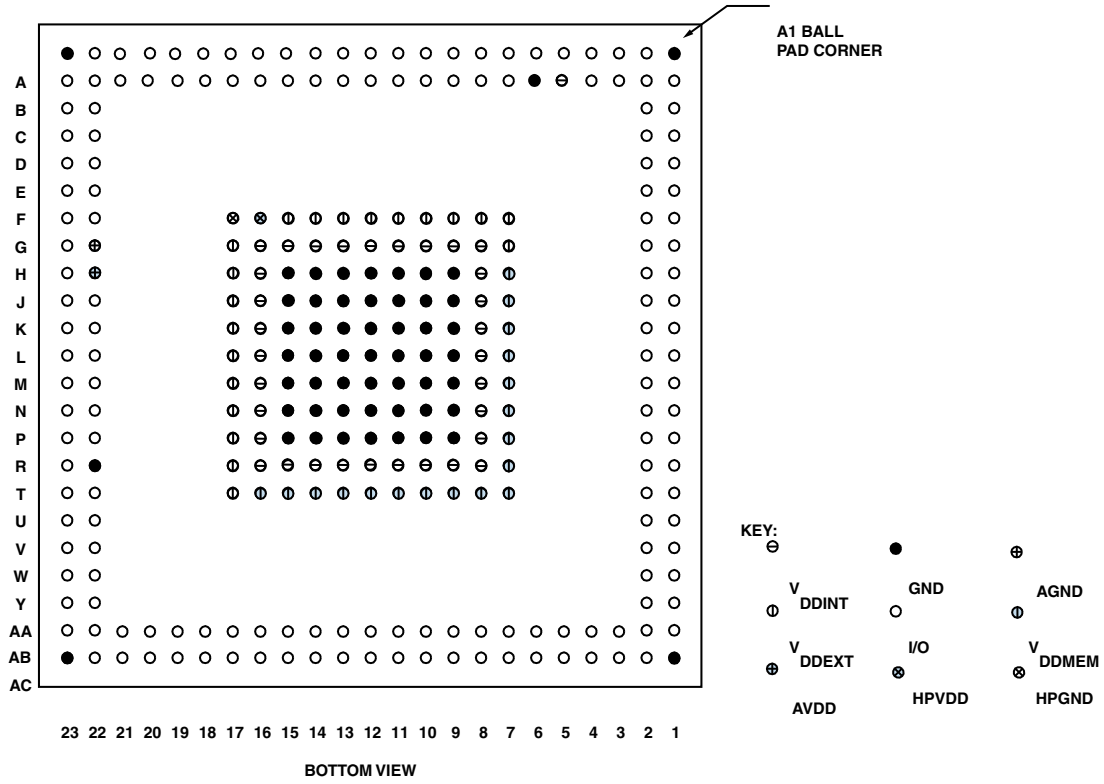

Figure 36. 289-Ball Mini-BGA Ball Configuration (Bottom View)

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Model	Temperature Range[1]	Package Description	Package Option	Instruction Rate (Max)	Operating Voltage (Nom)
ADSP-BF527KBCZ6C1X	0°C to +70°C	289-Ball Chip Scale Package Ball Grid Array (Mini-BGA)	BC-289	600 MHz	tbd V internal, 1.8 V or 3.3 V I/O

[1] Referenced temperature is ambient temperature.

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